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# SPACE ULTRARELIABLE MODULAR COMPUTER (SUMC) INSTRUCTION SIMULATOR: FINAL REPORT

Ву

R. T. Curran

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Prepared for

## NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

George C. Marshall Space Flight Center

Marshall Space Flight Center, Alabama

CONTRACT NAS8-26698

November 1972

CSC COMPUTER SCIENCES CORPORATION

# SPACE ULTRARELIABLE MODULAR COMPUTER (SUMC) INSTRUCTION SIMULATOR: FINAL REPORT

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R. T. Curran W. A. Hornfeck

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> COMPUTER SCIENCES CORPORATION 8300 South Whitesburg Drive Huntsville, Alabama 35802

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#### **FOREWORD**

The work reported herein was administered in the Applications Development Branch, Computation Laboratory, Marshall Space Flight Center with Mr. Bobby C. Hodges assigned as COR. In addition to his duties as Technical Monitor, Mr. Hodges added to our insight of the development problem through careful planning and coordination.

Acknowledgement is due Mr. Thomas E. Hill, also of the Applications Development Branch, for his many useful suggestions toward the integration of the simulator into the SUMC Support Supervisory System.

Cognizant Astrionics Laboratory personnel contibuted significantly to our understanding of the SUMC design specifications.

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#### SECTION I. INTRODUCTION

This report presents the description, design principles, functional operation, and recommended expansion and enhancements for the Space Ultrareliable Modular Computer (SUMC) interpretive simulator. Included in the appendices are the User's Manual, descriptions of machine instructions for the SUMC being modeled, Program Module Descriptions, Simulator Source Program listings, and a sample program printout.

Within the description of the simulation target computer, the basic architecture is discussed in terms of its effect on the simulator software organization. This section also includes a discussion of the instruction set which is executed under the initial simulator implementation as well as planned additions to this target instruction set.

The functional operation of the SUMC simulator is described according to basic operational modules which include the primary control loop, initialization, instruction parse and execute subroutines, user diagnostic aids, program termination, and interrupt simulation routines. In discussing the operation of the simulator, the key problems of host computer independence and target computer architectural scope are brought into focus.

A section is also included outlining recommended simulator expansion and enhancements. Simulation of input/output operations, expansion of the target instruction set, execution efficiency, and simulation of interrupt servicing operations are the topics discussed in this section.

#### SECTION II. GENERAL DESCRIPTION OF SUMC

#### A. SUMC Architecture

A simplified block diagram of the Space Ultrareliable Modular Computer (SUMC) is shown in Figure II-1. The Arithmetic Logic Unit (ALU), Main Memory Unit (MMU), Scratch-Pad Memory (SPM), Control Unit (CU) and Multiplexer/Register Unit (MRU) are the five basic functional units of the SUMC. The Floating-Point Unit (FPU) is a sixth basic unit; however, a particular SUMC configuration may or may not include the FPU. Modular construction of the SUMC allows the computer word length to be varied, in four-bit increments, to satisfy specific space mission requirements. For this application, the SUMC simulator models a target computer having a 32-bit word length and no floating-point arithmetic capability, i.e., the SUMC configuration does not include the FPU and only fixed-point arithmetic instructions may be processed.

Figure II-2 depicts a detailed block diagram of the SUMC with the basic functional units broken down into their major components. The Arithmetic Logic Unit (ALU) accepts inputs from the Floating-Point Multiplexer (FPM), SPM, I/O Unit, Microprogram Read-Only Memory (MROM), and Memory Register (MR). The Control Unit (CU) enables the appropriate multiplexer, depending on the instruction. The Add/Sub Units can perform an add, subtract, reverse subtract, logical AND, logical OR, logical EXCLUSIVE OR, 1's complement and 2's complement. The correct function is enabled by a signal from the Control Unit (CU), depending on the instruction.

The Multiplexer/Register Unit (MRU) accepts data from the ALU, SPM, I/O Unit, and FPU. The Product/Remainder Multiplexer (PRM) can accept data from the ALU, force zeros out, shift ALU data right one, left one, left two, right four, and left four. The Memory Address Multiplexer (MAM) gates data or zeros to the memory address register (MAR) from the ALU or MAR. The MAM can shift data right one, left one, left two, right four, and left four. The Multiply Quotient Multiplexer (MQM) gates data or zeros

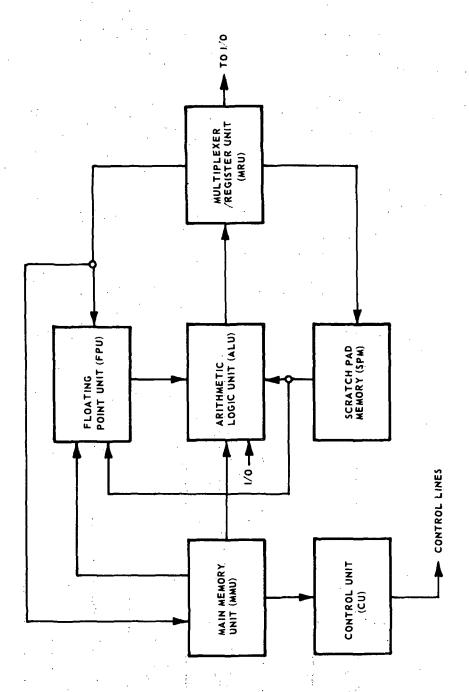


FIGURE II-1 SIMPLIFIED SUMC SYSTEM BLOCK DIAGRAM.

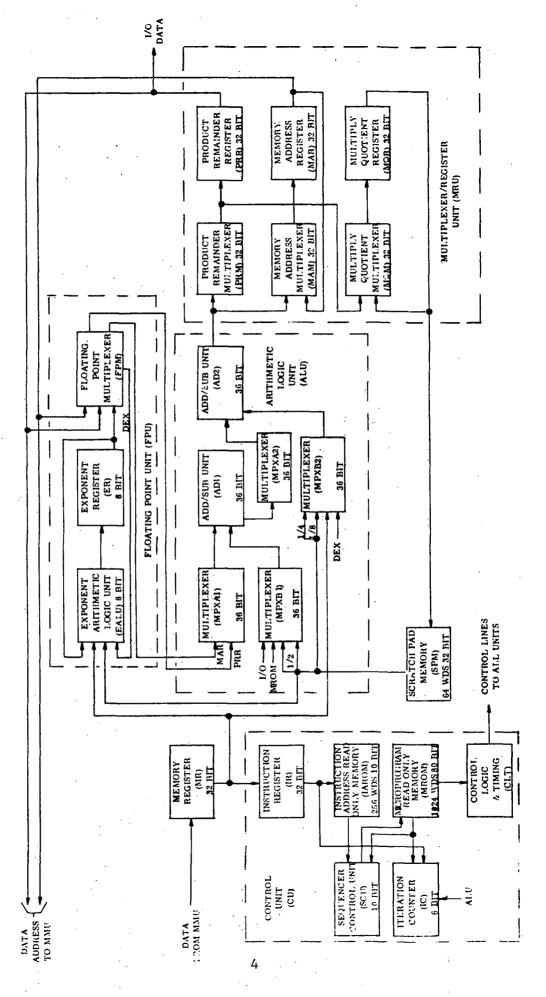


Figure II-2 Detailed SUMC System Block Diagram

to the Multiply/Quotient Register (MQR) from the PRM or MQR. The data from the MQM can be shifted left one, left two, and right four. The MQR sends data to the MQM or SPM. The registers and multiplexers in the MRU are controlled by microinstruction signals from the Control Unit and allow data from the ALU to be gated through the multiplexers and clocked into various registers.

The Scratch Pad Memory (SPM) contains program addressable registers, current Program Status Word (PSW), and temporary storage area. The SUMC breadboard system, which acts as the current target computer, contains a 64-word, 32-bit scratch pad memory. The SUMC breadboard SPM contains 16 General Registers, eight Floating-Point Registers, program counter, a system mask word, a program mask word, condition code bits, protection key word and program state word. The SPM layout is shown in Figure II-3. The function of the SUMC SPM is to send data to the ALU and accept data from the MRU while controlled by microinstruction signals from the Control Unit.

The Floating-Point Unit (FPU) is a special logic section which enhances the execution of floating-point instructions. The current version of the SUMC simulator has not been designed to include floating-point capabilities and a discussion of the FPU will not be presented here.

The Control Unit (CU) decodes SUMC instructions and provides micro-instruction control signals for the ALU, SPM, MMU, MRU, and FPU as required to execute the current instruction. This unit is made up of a number of distinct components and each of these is discussed briefly in the following paragraphs.

Instruction Register (IR) - This 32-bit register is used to hold the instruction which is currently being executed. The op code portion of the IR is used as an address for the IAROM.

Instruction Address Read-Only Memory (IAROM) - The IAROM is a 64-word, 12-bit read-only memory which contains the starting address of the microinstruction sequence stored in the MROM which will perform the machine instruction. The content of the IAROM, whose address is specified by the instruction op code, is gated to the Sequencer Control Unit.

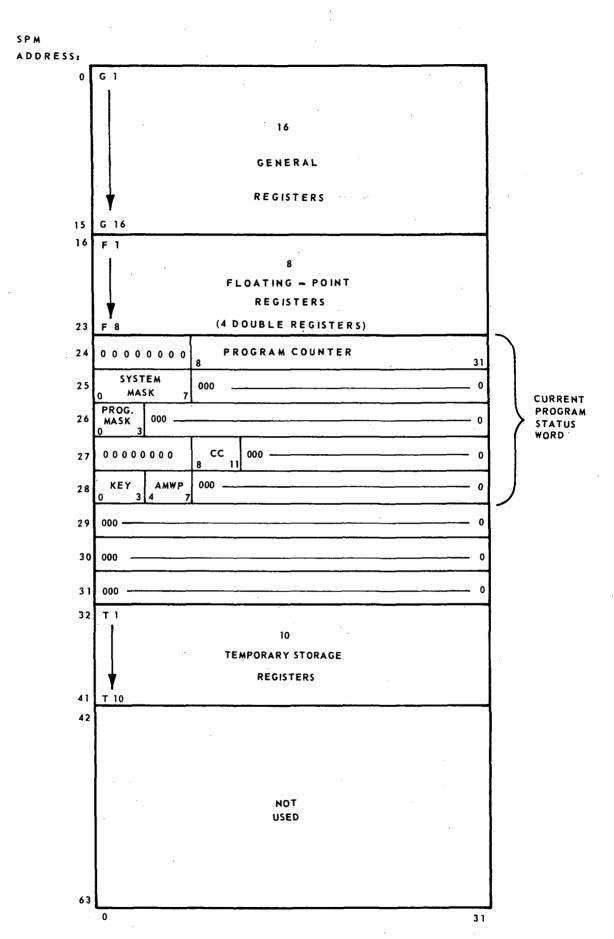


FIGURE 11-3. SUMC BREADBOARD SYSTEM SCRATCH PAD MEMORY MAP.

Sequencer Control Unit (SCU) - The sequencer serves as an address register for the microprogrammed read-only memory. The ten-bit sequencer register can be loaded from the IAROM, MROM, or the ALU.

Microprogram Read-Only Memory (MROM) - The MROM is 1024-word, 72-bit read-only memory containing a prestored sequence of microinstructions required to fetch and execute the program instructions, initiate and control I/O operations, and respond to external interrupts. An instruction is executed by broadcasting a location or a sequence of locations of the MROM to the ALU, SPM, MRU, FPU, and main memory.

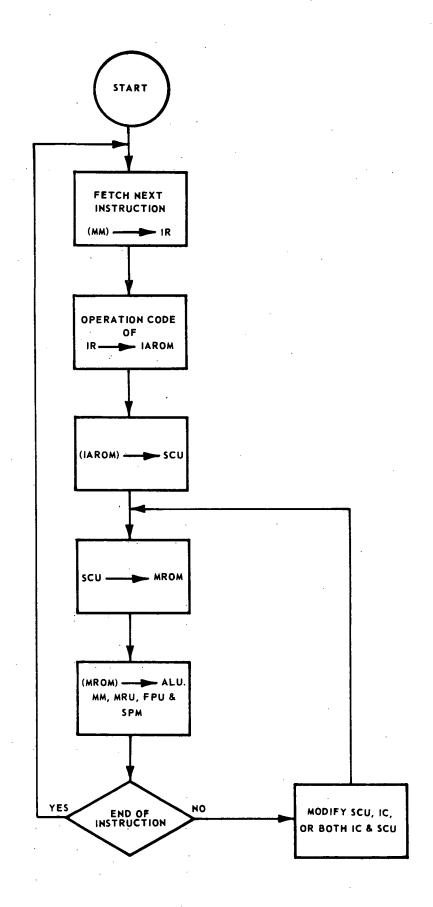
Iteration Counter (IC) - The IC is used to control the number of times a single or a sequence of microinstructions in the MROM should be repeated. The six-bit IC register can be loaded from the IR, ALU, and MROM.

Figure II-4 is a flow chart which depicts the sequence of operations performed by the Control Unit in executing an instruction. More detailed explanations of the operating of the SUMC Control Unit as well as other SUMC architectural features can be found in appropriate literature (1), (2), (3), (4), pertaining to SUMC hardware characteristics. The preceding discussion is intended to relate only the basic principles of SUMC architectural design and the source of the material has been the <u>SUMC Breadboard System Operations Guide</u> (1).

#### B. SUMC Instruction Set

The SUMC breadboard system is a 32-bit byte-oriented machine which performs arithmetic operations that fall into four classes: fixed point and logical arithmetic, floating-point arithmetic, character manipulation, and I/O operations. The fixed-point and logical arithmetic operations require the following data types:

- Half-word fixed-point number
- Full-word fixed-point number
- Fixed-length logical information



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FIGURE II-4. SUMC CONTROL UNIT (CU) FLOW DIAGRAM

The floating-point arithmetic operations require:

- Short floating-point number
- Long floating-point number

The character manipulation operations require:

- Packed decimal number
- Zoned decimal number
- Variable-length logical information

Figure II-5 shows the data formats for the eight different types of data mentioned above. The SUMC simulator is presently concerned with six of the eight data types in that floating-point capabilities will be added to the program at a later time.

The SUMC breadboard system uses instruction formats which may be one, two, or three half-words in length. A total of five different instruction formats are used:

- RR register-to-register operation format
- RX register-and-indexed-storage operation format
- RS register-and-storage operation format
- SI storage-and-immediate-operand operation format
- SS storage-to-storage operation format

The instruction formats are shown in Figure II-6 along with a brief description of the different fields of each instruction. In describing the execution of instructions, operands are designated as first, second, and third operands according to the manner in which they participate. The operand to which a field in an instruction format applies is denoted by the number following the code name of the field.

Table II-1 lists the instruction set which has been implemented for the SUMC breadboard system simulator. This table contains the instruction op codes, their corresponding mnemonics, and appendix page numbers referring to the instruction description. As mentioned previously, there are four types, or groups, of instructions and the present version of the simulator will interpretively execute SUMC programs for the breadboard

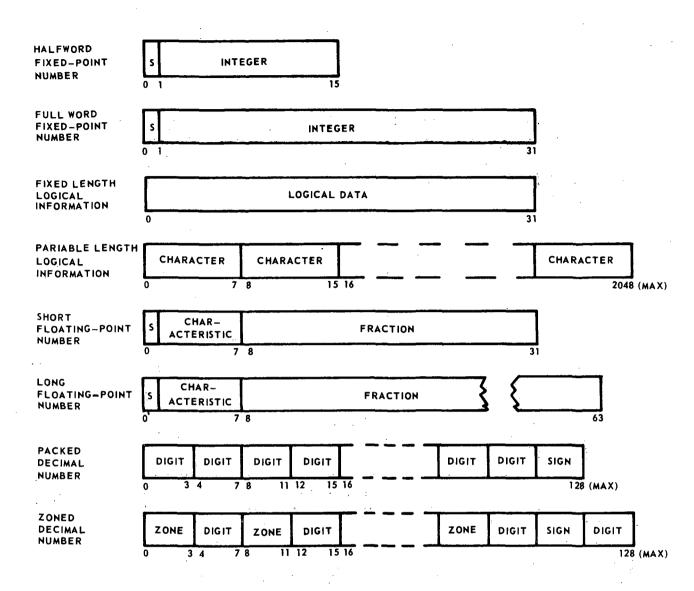
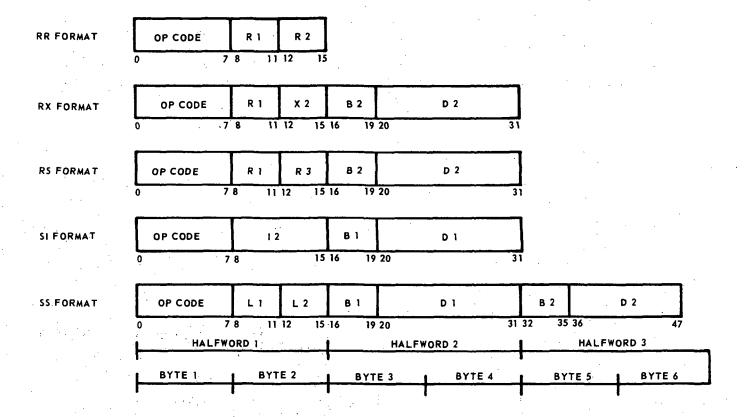


FIGURE 11-5. SUMC BREADBOARD SYSTEM DATA FORMATS.



#### OP CODE - ISTR INSTRUCTION OPERATION CODE

- R 1 REGISTER OPERAND 1 SPM ADDRESS
- R 2 REGISTER OPERAND 2 SPM ADDRESS
- R 3 REGISTER OPERAND 3 SPM ADDRESS
- X 2 OPERAND 2 INDEX REGISTER SPM ADDRESS
- B 1 OPERAND 1 BASE REGISTER SPM ADDRESS
- B 2 OPERAND 2 BASE REGISTER SPM ADDRESS
- D 1 OPERAND 1 DISPLACEMENT ...
- D 2 OPERAND 2 DISPLACEMENT
- 12 IMMEDIATE OPERAND 2
- L 1 OPERAND 1 LENGTH SPECIFICATION
- L 2 OPERAND 1 2 LENGTH SPECIFICATION

#### FIGURE 11-6. SUMC BREADBOARD SYSTEM INSTRUCTION FORMATS.

Table II-1. Instruction Set for the SUMC Breadboard System Simulator

Group I. Standard (Fixed-Point) Instructions

Code	Mnemonic	Page	Code	Mnemonic	Page	Code	Mnemonic	Page
04	SPM	III-2	40	STH	III-6	. 80	SSM	III-13
05	BALR	III-2	41	LA	III-6	82	LPSW	III-13
06	BCTR	III-2	42	STC	III-7	86	BXH	III-13
07	BCR	III-2	43	IC	III-7	87	BXLE	III-13
OA	SVC	III-3	44	EX	III-7	88	SRL	III-14
			45	$\mathtt{BAL}$	III-7	89	SLL	III <b>-</b> 14
10	LPR	III-3	46	BCT	III-8	8A	SRA	III-14
11	LNR	III-3	47	BC	III-8	8B	SLA	III <b>-</b> 14
12	LTR	III-3	48	LH	III-8	. 8C	SRDL	III-15
13	LCR	III-3	49	CH	III-8	8D	SLDL	III <b>-</b> 15
14	NR	III-4	4A	HA	III-9	8E	SRDA	III <b>-</b> 15
15	CLR	III-4	4B	SH	III <b>-</b> 9	8 <b>F</b>	SLDA	III <b>-</b> 15
16	OR	III-4	4C	MH	III-9			
17	XR	III-4	4E	CVD	III-9	90	STM	III <del>-</del> 16
18	LR	III-4	4F	CVB	III-10	91	TM	III-16
19	CR	III-5				92	MVI	III-16
1A	AR	III-5	50	ST	III-10	93	TS	III <b>-</b> 16
1B	SR	III-5	54	N	III-10	94	NI	III <b>-</b> 17
1C	MR.	III-5	55	$\mathtt{CL}$	III-10	95	CLI	III-17
1D	DR	III-5	56	0	III-10	96	OI	III-17
1E	ALR	III-6	57	$\mathbf{X}_{j}$	III-11	97	XI	III-17
1F	$\mathtt{SLR}$	III-6	5 <b>8</b>	L	III-11	98	LM	III-17
		• •	59	С	III-11			
			5A	A	III-11			
			5B	S	III-11			
		*	5C	M	III-12		•	
		•	5D	D	III-12			
			5E	AL	III-12			
			5F	SL	III-12			

Group III. Character Manipulation Instructions

Code	Mnemonic	Page	Code	Mnemonic	Page
D1	MVN	III <b>-</b> 19	F1	MVO	III-21
D2	MVC	III-19	F2	PACK	III-21
D3	MVZ	<b>III-</b> 19	F3	UNPK	III-22
D4	NC	III-19			
D5	CLC	III-20			• •
D6	OC	III-20			
D7	XC	III-20			
DC	TR	III-20			
DD	TRT	III-21			

system which contain any of the Group I or Group III instructions of Table II-1.

Appendix II describes the execution of the Group I and Group III instructions as they are processed by the SUMC breadboard system and simulated by the SUMC interpretive simulator.

#### SECTION III. THE SUMC INTERPRETIVE SIMULATOR

#### A. Design Principles

1. <u>Host Computer Independence</u>. One of the primary design goals for the interpretive simulator is the capability to simulate the operation of the SUMC family of machines on a variety of host computers. To accomplish this, great care has been taken to identify all host-machinedependent operations which must be performed during a simulation.

The need to design a host computer independent simulator has been dictated by two considerations. First, and probably more important, the resulting program would be valuable to a larger cross-section of users if the problem of transferring the simulator between host computers is not a major or costly undertaking. Secondly, the development effort may be done on whichever machine may be practical or available (in this case, an IBM 7094) and the finished simulator is then easily converted for use on other host systems (in this case, a Univac 1108).

The choice of an appropriate simulator source language was influenced strongly by the desirability of maintaining host computer independence. The standard FORTRAN IV source language was chosen for the simulator since it represents a high-level language which is common to most large-scale computer systems. Although a higher-level language would have eased programming efforts, it was decided that the machine-independence criterion was of overriding importance. It has been recognized that certain FORTRAN IV processing characteristics will vary from one system to the next; however, these have been noted and appropriate coding is used to circumvent this problem.

The requirement for program transfer among several computer installations has led to a highly modular program structure. The simulator has thus been constructed as a set of quasi-independent modules, regulated by a control module, as shown in Table III-1. This table includes all program modules which are presently included in the basic simulator package and those modules which are not completely machine independent are

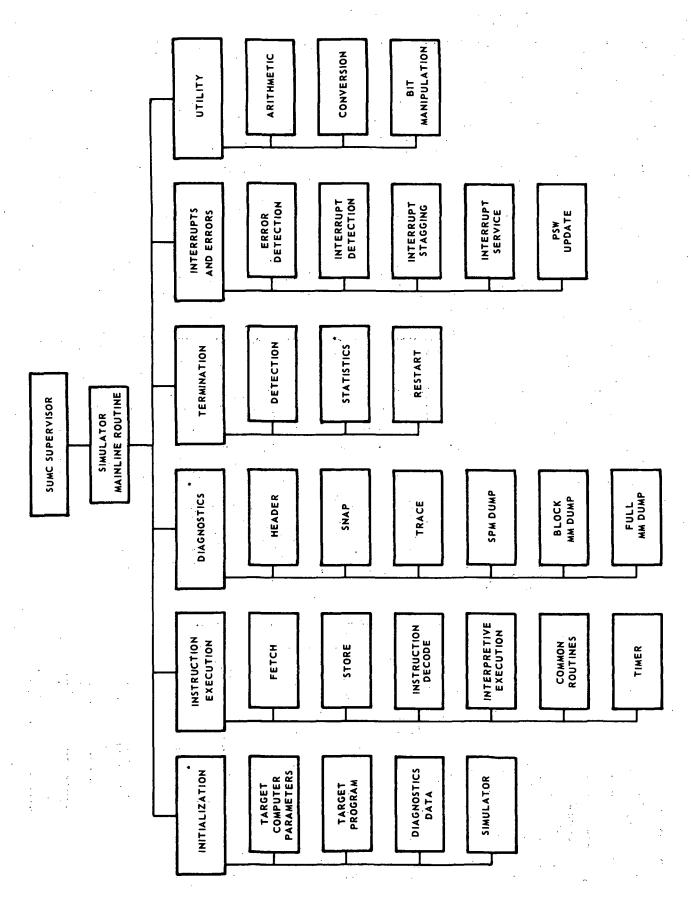


TABLE III-1. BASIC SUMC SIMULATOR MODULES.

marked with an asterisk. Table III-2 gives a brief description of the function of each program module. Transfer of the simulator among host computers would therefore require modifications or replacement of only those modules marked in the figure.

There are three primary areas of programming for the simulator in which differences in host computer characteristics had a noticeable effect. These are:

- host computer word length
- host computer arithmetic
- host computer I/O procedures

Problems encountered in each of the above areas have been resolved such that the simulation package is machine independent to the fullest possible extent.

- a. Word Length. The possibility of a variation in host computer word length when transferring the simulator between host systems is a readily apparent problem. A parameter, IHOST, specifying the host computer word length has therefore been introduced as a common variable in appropriate simulator subroutines. The IHOST variable is initialized along with other standard program variables prior to start of a simulation.
- b. Arithmetic. The SUMC target computer employs two's-complement arithmetic exclusively. However, a given host computer may be a two's-complement, one's-complement or sign-magnitude machine. The following possibilities are therefore reasonably likely:
  - 2's-complement target computer & 2's-complement host
  - 2's-complement target computer & 1's-complement host
  - 2's-complement target computer & sign-magnitude host

In the first case, when both target and host computers employ 2's-complement arithmetic, simulation of target computer operations is straightforward and conversion problems are not present.

In the two latter cases, however, proper conversions must be made during simulation since arithmetic quantities are represented differently in host and target systems. The present version of the SUMC simulator

Table III-2. Simulator Module Definitions

	Program Modules	Function Summary
	A. INITIA	ALIZATION
1.	Target Computer Parameters	Input values for host and target computer architectural parame-
2.	Target Program	ters. Input target computer memory
3.	Diagnostics Data	map. Input diagnostics keys and cor- responding numerical data for diagnostic control.
4.	Simulator Variables	Input internal simulation parameters.
	B. INSTRUCT	ION EXECUTION
1.	Fetch	Fetch instructions and data from simulated main memory.
2.	Store	Store instructions and data in simulated main memory.
3.	Instruction Decode	Parse current instruction and represent contents as FORTRAN
1.	Tatana matina Rasantian	variables.
4. 5.	Interpretive Execution Common Routines	Process current instruction.  Arithmetic processing common to several instruction routines.
6.	Timer	Maintains records pertaining to program simulated elapsed time.
	C. DI	AGNOSTICS
1.	Header	Information printed to identify diagnostic output.
2.	Snap	Check and execute SNAP diagnostic
3.	Trace	Check and execute TRACE diag- nostic.
4.	SPM Dump	Check and execute SPM DUMP diagnostic.
5.	Block MM Dump	Check and execute BLOCK MM DUMP diagnostic.
6.	Full MM Dump	Check and execute FULL MM DUMP diagnostic.
	D. TER	MINATION
1.	Detection	Detect program termination condi- tions.
2.	Statistics	Collect and print end-of-run statistics.
3.	Restart	Collect restart data.

Table III-2. Simulator Module Definitions (Continued)

Program Modules		Function Summary
	E. INTERRU	PTS AND ERRORS
1. 2.	Error Detection Interrupt Detection	Detect and flag error conditions.  Detect and identify interrupt  conditions.
3.	Interrupt Stacking	Maintain stack of pending inter- rupts.
4.	Interrupt Service	Process pending interrupts at appropriate times according to predetermined priorities.
5.	PSW Update	Maintain old and new program status words in simulated MM and SPM
	. F.	UTILITY
1.	Arithmetic	Perform generic arithmetic operations.
•	Conversion	General conversion routines.
3.	Bit Manipulation	Perform generic bit manipulation operations.

is operational on the IBM 7094 system which is a sign-magnitude machine. Two special (host machine dependent) routines are therefore present - ITWTSM, for conversion of 2's-complement data to sign-magnitude representation, and ISMTWO, for conversion of sign-magnitude to 2's-complement representation. Prior to simulation of a particular SUMC operation, appropriate target computer data must be converted to host machine form using the ITWTSM routine. Following the simulated operation, which is performed under host machine arithmetic, the results are converted to target machine form using the ISMTWO routine. It should be noted here that performing arithmetic operations using an arithmetic base other than that of the host machine would be prohibitive from an efficiency standpoint. Thus, the conversion routines are necessary.

Transfer of the simulator to a Univac 1108 operating environment would of course require appropriate conversion routines in order to perform arithmetic operations using the host computer 1's-complement representation. Substitution of the different conversion routines can be done with a minimum of difficulty.

c. I/O Operations. The most difficult problem encountered in achieving a truly machine independent simulator has been in the area of host machine Input/Output operations. That is, I/O processing characteristics are highly dependent on the particular choice of host computer. For this reason, all simulation procedures which require the utilization of host computer I/O operations have been segregated so that extensive I/O revisions are not necessary when transferring the simulator between host computers.

Host computer I/O operations are necessary during four distinct simulation phases:

- Initialization
- Diagnostics
- Termination
- Interrupt servicing

During initialization, the host computer must input the target computer memory map as well as the various target machine and host machine parameters which are needed for simulation. All READ operations which are performed by the host computer are included in the subroutine INITLZ. This routine handles the initialization operations at the start of each simulation and must input the following:

- Target computer main memory map
- Target computer SPM map
- Target computer architectural parameters
- Host computer architectural parameters
- Simulation control variables
- Diagnostics variables

This routine is written in standard FORTRAN IV for processing on the IBM 7094. Operation on another host machine could of course require modification or replacement of INITLZ.

The simulator includes a number of diagnostic features which require both READ and WRITE operations to be performed by the host computer. Since the simulation diagnostic aids are designed primarily for target computer debugging and verification in the environment of a commercially available system, the applicable routines are inherently host machine dependent to a certain extent. However, by coding these routines in the standard FORTRAN IV source language and circumventing host computer dependencies where possible, the modifications required for switchover to a different host system are not major ones.

Several host machine I/O operations are required at the termination of a simulation run. These are WRITE operations which may be any of the following:

- error messages
- statistical dumps
- target memory dumps
- diagnostics information

Each of the above output operations have been coded using distinct subroutines and standard FORTRAN IV source language. Relatively few lines of code are needed for these operations which allows subroutines that are easily transferable between host systems.

The Interrupt Service routines have not been finalized for the IBM 7094 version of the simulator. Some machine dependencies exist in the present scheme; however, it is hoped that the final version of the simulator will feature interrupt processing simulation which is completely host machine independent.

2. Target Computer Architectural Scope. The basic interpretive simulator, as presently configured, operates on an IBM 7094 host system and has the capability to model a SUMC family of target machines. This section will be devoted to a discussion of the SUMC characteristics and design parameters which may vary under the present simulation program. Flexibility has been designed into the simulator so that an even wider range of target machines may eventually be modeled through future enhancements to the basic program. These possibilities are also discussed in this section.

The simulator has been designed such that changes in the following SUMC architectural features can be accommodated presently or with little additional modification.

- SUMC word length
- main memory size
- scratch-pad memory size
- scratch-pad memory organization
- microprogram read-only-memory contents
- addition of floating-point arithmetic unit
- I/O devices
- interrupt response routines

The present version of the SUMC simulator is capable of adjusting to variations in several of the above features. Planned enhancements in the remaining areas will allow the simulation of a widely varying group of target computers. The present allowable architectural scope of the SUMC target computer, in terms of the above mentioned features, will be described here in detail.

a. SUMC Target Computer Word Length. The current version of the SUMC simulator is intended to model a target computer having a word

length of 32 bits. However, the program can be readily modified to simulate a similar SUMC computer having a smaller word length. The allowable word lengths vary from a minimum of 16 bits to the present 32 bits, with the restriction that the word length be a multiple of four. This restriction is certainly reasonable since the SUMC has been designed as a fourbit modular computer. The target computer word length is a simulation parameter in the form of a COMMON variable called ITARG, which may be initialized by the user at the start of a simulation.

- b. SUMC Target Computer Main Memory Size. A variation in the size of the target computer main memory is certainly a very likely possibility. Provision has been made for this occurrence in the present version of the SUMC simulator. The number of addressable locations in the SUMC main memory is specified for the simulation program via the DIMENSION statement for the array IMAINM. The size of simulated target main memory can then be changed by modification of the IMAINM array dimension statement in each appropriate subroutine or subprogram. The IMAINM array contains the current contents of simulated SUMC main memory throughout the simulation. The number of addressable locations which may be simulated for the SUMC main memory varies from a minimum of 128 locations to a maximum of 32,768 locations.
- c. SUMC Target Computer SPM Size. As in the case of target computer main memory size, SUMC scratch-pad memory size is likely to vary. In the present version of the simulator, SPM registers are simulated as an array called ISPM, which contains the current contents of the target computer SPM in SUMC format. If the number of registers contained in SPM should change for a particular target computer, a simple change in the dimension statement for the ISPM array will effect a corresponding change in the simulation program. The present SUMC target machine utilizes a SPM which contains 64 registers. This represents the minimum number of SPM words which are anticipated for a particular target computer configuration. Any reasonable increase in the target computer SPM size could be handled under the present program.
- d. SUMC Target Computer SPM Organization. Figure II-3, which is referred to in a previous section, describes the SUMC SPM layout

which is used for the current target computer. It basically consists of:

- General registers
- Floating point registers
- Status registers
- Temporary storage registers
- Spares

Due to the fact that the component parts of Scratch Pad Memory as well as their organization may vary from one SUMC application to the next, the SUMC simulator has been designed with considerable flexibility in this respect.

- (1) General Registers This group of registers is made up of accumulators, base registers, index registers, and general purpose registers. The present design philosophy is to allow each of the general registers to be used as an accumulator, base register, or index register. That is, a contiguous block of 16 general purpose registers. In addition, this block of registers may occupy any 16 continuous SPM locations. A particular general register is addressed by adding an offset from zero to the instruction register address, with the offset being a simulation parameter initialized by the user.
- (2) Floating Point Registers The simulator currently contains no provisions for executing floating point instructions and therefore does not allocate SPM registers for floating point operations. The problem of register storage for floating point arithmetic will be addressed when a final version of the SUMC simulator is implemented.
- (3) Program Status Word (PSW) Target computer program control and linkage is accomplished through a number of program status words, as in the IBM 360 machine. Under this scheme, the current program status word resides in scratch pad memory in the form of a group of status registers. For the simulator, all status words used in controlling the target computer are present in the form of COMMON variables. In assigning SPM locations for the status information, each simulation variable, which is actually part of the overall program status word, is made

equivalent to its desired SPM location. To change the layout of the PSW in scratch pad memory, an appropriate change in each applicable EQUIVALENCE statement is necessary.

- (4) Temporary Storage Registers Ten temporary storage registers are included in the target SUMC SPM layout. The number and location of these registers may be varied in the current version of the SUMC simulator. The temporary registers are assigned to elements of the ISPM array using FORTRAN EQUIVALENCE statements and appropriate modifications of these statements will adjust the ISPM layout accordingly.
- (5) Spares Any SPM registers which remain unused for a given scratch pad layout are included in this category and are inconsequential to simulator operations.

Table III-3 lists the critical SUMC design parameters which may vary according to the particular target computer under consideration. Minimum and maximum values permitted for each parameter are given along with incremental variations which are allowed. Table III-4 lists the values which are currently assumed for the SUMC target computer and have been implemented in the initial version of the simulator.

- e. SUMC Target Computer MROM. SUMC instruction execution is controlled by signals from the microprogrammed read-only memory. Any additions, deletions, or modifications which are made to the instruction set of the target computer are implemented through a change in the applicable microcode. The SUMC simulator, in a similar manner, performs interpretive instruction execution by means of FORTRAN subroutines and, therefore, changes in the instruction set of the target computer are transformed into modifications in the appropriate subroutine. The present version of the simulator performs all actual instruction execution operations with the OPDEF subroutine and instruction set changes would, in most cases, involve only this particular subroutine.
- f. SUMC Target Computer Floating Point Arithmetic. No floating point arithmetic instructions have been implemented for this version of the SUMC simulator. The addition of floating point arithmetic capability is planned as one of the early enhancements to the basic simulator.

Table III-3. Critical SUMC Architectural Parameters

Parameter	Minimum	Maximum	Increment
Word Length (bits)	16	. 32	4
SPM Size (words)	16*	256	
Accumulators	1	16	1
Base Registers	1	16	1
Index Registers	1	16	1
General Registers	0	16	1
MM Size (locations)	128*	32,768	-

<sup>\*</sup>The minimum is shown for illustrative purposes and is not considered to be a critical value.

Table III-4. Current SUMC Design Parameters

	Parameter	Value	
	Word Length (bits)	32	Ī
	SPM Size (words)	64	
	Accumulators	0	
	Base Registers	0	
	Index Registers	0	•
1:, .	General Registers	16	
	MM Size (locations)	4,096	

g. SUMC Target Computer Interrupts. The interrupt scheme associated with a given target computer will in general be unique to that particular machine. This dependence of the interrupt action on the target computer results in an interruption package for the SUMC simulator which will vary greatly from one application to the next. An attempt has therefore been made to isolate all interrupt operations in the simulator within a few specific program modules.

The present SUMC target computer employs an interrupt scheme which is similar to that of an IBM/360 system, with certain exceptions. An interruption consists of storing the current PSW as an old PSW and fetching a new PSW. Processing resumes in the state indicated by the new PSW. The old PSW contains the address of the instruction that would have been executed next if an interruption had not occurred and the instruction-length code of the last interpreted instruction.

The interruption action for the target computer will differ from IBM/360 operation in the following respects:

- Interrupts occur from just a single I/O channel.
- External interrupts originate only from the operator interrupt key.
- No decimal arithmetic program interruptions.
- No protection exception program interruption.

With the exception of the above differences, interrupt processing for the SUMC target computer will parallel that of the IBM/360 system.

The simulator presently is capable of detecting all target computer interrupt conditions and will notify the user of their presence. Interrupt response or service routines have not been implemented for this version of the simulator but are planned for inclusion at a later date. A detailed explanation of all interrupt conditions which are detected and the program action which is taken will be given in a later section of this report.

h. SUMC Target Computer I/O. The SUMC simulator does not provide for simulation of input/output operations performed by the target

computer. Actual simulation of I/O operations will be performed by I/O device simulation routines which will be written for each individual application. Another section of this report, which covers future enhancements and expansion of the SUMC simulator, will describe in further detail a proposed I/O simulation scheme which could be added to the basic simulator at a later time.

# B. Functional Operation

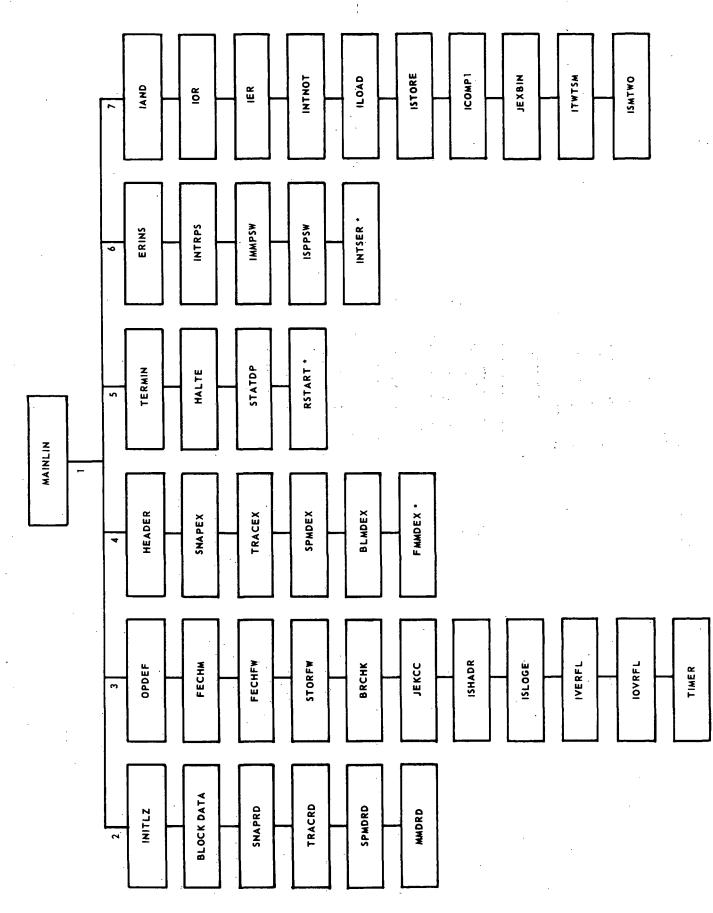
The SUMC interpretive simulator has been designed in a stand-alone, highly modularized fashion with a single supervisor module, MAINLIN, controlling all simulation sequencing. As shown in Figure III-1, the subroutines which operate under control of MAINLIN are divided into six areas:

- Initialization routines
- Instruction fetch and execute
- Diagnostics routines
- Termination routines
- Interrupt servicing
- Utility routines

Although there are no restrictions within the basic simulator package concerning CALLING and CALLED subroutines, the basic cycling of operations which are performed to interpretively execute each instruction is controlled in a macro sense by the MAINLIN program.

The simulation process performed by the complete set of program modules, under control of MAINLIN, is functionally self-contained for present operation in the IBM/7094 development environment. However, the SUMC simulator will ultimately become part of a larger set of programs devoted to support of the SUMC family of computers as shown in Figure III-2, Integration of Simulator into SUMC Support Software. This report will describe the functional operation of the simulator in its present form as an independent programming system.

1. <u>Primary Control Loop</u>. As mentioned in the previous section and shown in Figure III-1, the basic control for the simulator is provided



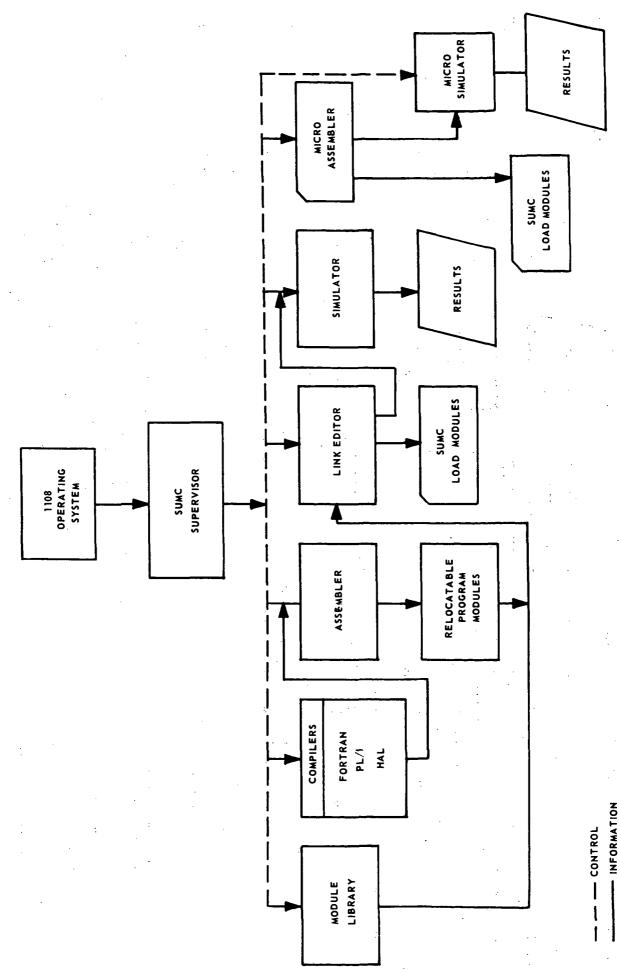


FIGURE III-2, INTEGRATION OF SIMULATOR INTO SUMC SUPPORT SOFTWARE

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by the MAINLIN program. The simulation process is carried out, under control of MAINLIN, in the following primary phases:

- Input of Job Description
  - host computer parameters
  - target computer parameters
  - diagnostics control variables
  - target computer memory map
- Interpretive Execution of Target Program
  - interruption action
  - fetch and decompose next target instruction
  - perform diagnostics requested
  - execute instruction and update timer
  - error termination or process next instruction
- Termination of Program
  - printout of requested results and/or error message
  - exit

A flow diagram of the MAINLIN routine is shown in Figure III-3. The initial action taken by the program is to dimension all necessary variables and define the program COMMON area. The simulation initializer routine, INITLZ, is then called in order to input the necessary simulation parameters, diagnostics keys, and target program.

If the simulator has been properly initialized, the error flag remains set at zero and the program begins the interpretive execution of target program instructions in the following steps.

- a. If the interrupt counter is at zero, there are no interrupts pending from a previous instruction and control is transferred to the simulated fetch cycle. If any interrupts are pending, they are serviced according to a predetermined priority. Interrupt servicing will be handled by subroutine calls controlled by interrupt keys.
- b. After all pending interrupts have been serviced, the next instruction is fetched from simulated target main memory by the FECHM

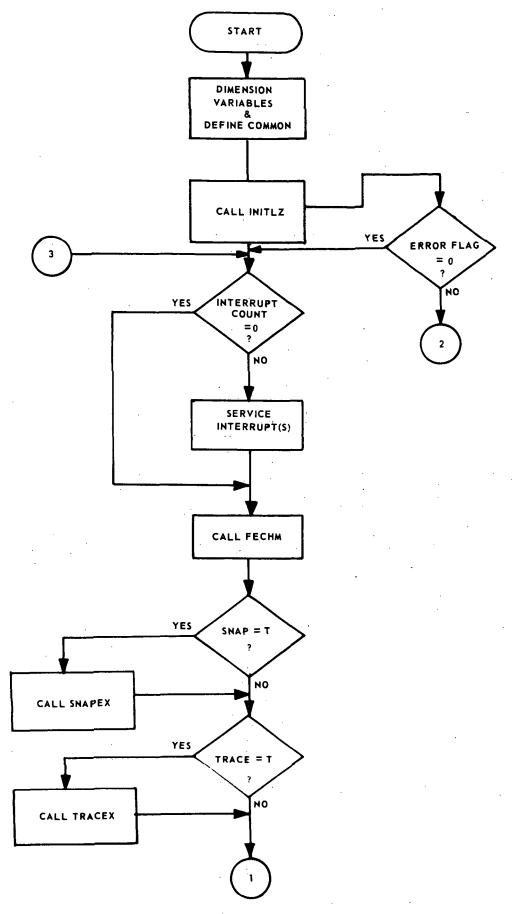


FIGURE III-3. FLOW DIAGRAM OF MAINLIN PROGRAM

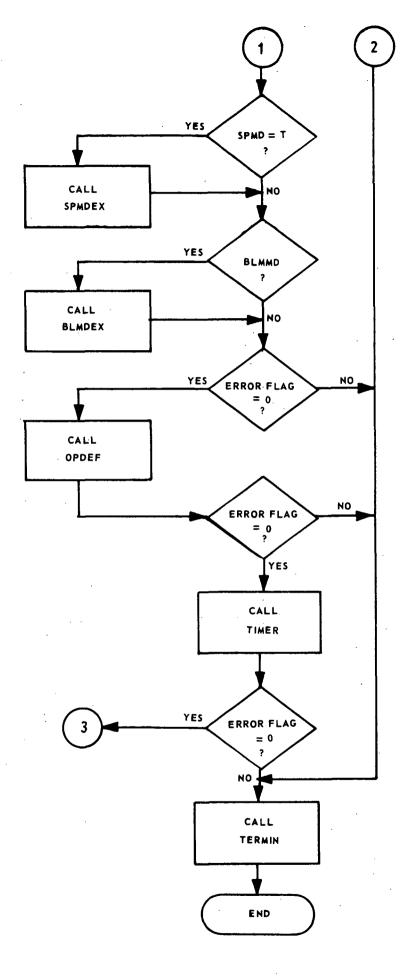


FIGURE III-3 (CON'T) 32

routine. This subroutine obtains the proper instruction according to a simulated program counter. FECHM also parses the current instruction in order to transform all information contained in the instruction word into the form of FORTRAN variables usable by the simulator.

- c. The simulation error flag is checked again upon return from the FECHM subroutine and, if it remains zero, the program begins checking for user diagnostic requests. The four types of user diagnostics made available by the simulator are checked as follows:
- (1) If any main memory "snap" diagnostics have been requested by the user, the SNAPEX subroutine is called to execute the check. This routine checks all extant snap keys to determine whether the user desires data at this point in the program. If so, the appropriate data is collected for printout.
- (2) If any register traces have been requested, the TRACEX subroutine is called to execute the check. This routine checks all trace keys and collects appropriate data if a register trace is desired.
- (3) If a printout of scratch pad memory contents is desired at some time during the simulation, the SPMDEX routine is called at this point to check SPM dump keys which have been supplied by the user to trigger the diagnostic. If triggered, the current contents of all SPM registers are printed before executing further.
- (4) A printout of the contents of a particular block of contiguous main memory locations may be requested by the user at some point during the simulation. The BLMDEX subroutine is called to check keys used to trigger this dump. If triggered, a printout of the contents of the specified locations is executed by this routine.
- d. The program is now set up to perform the interpretive execution of the current instruction. The OPDEF subroutine is called for this purpose and subsequently performs arithmetic operations and data manipulation called for by the instruction. The interpretive execution of a target instruction must maintain the contents of all SUMC registers available to the target-computer programmer. In addition, the contents of

the simulated SUMC registers must duplicate, on a bit-for-bit basis, the contents of actual target computer registers under normal operation.

- e. If the simulator error flag remains set at zero upon return from the OPDEF subroutine, the TIMER routine is called for the purpose of updating simulated execution time.
- f. Following the return from the TIMER subroutine and another check of the error flag, the program returns to the interrupt detection loop and prepares to execute the next instruction.

At the termination of a simulation run, due to either (1) the execution of a target program HALT instruction or (2) the setting of the simulation error flag, the TERMIN subroutine is called. This routine presently handles post processing statistics printouts, but will also control collection of simulation restart data when this capability is implemented.

2. <u>Initialization</u>. The SUMC has been designed as a highly modular machine and is therefore capable of being configured in a number of different ways. This feature presents a unique problem in the simulation of such a machine in that quite a large number of target computer characteristics must be parameterized and input to the simulator as variables during initialization. These parameters involve both hardware and software aspects of the target computer which are subject to change from one application to the next.

The arrays which simulate SUMC scratch pad memory and main memory must be given their initial values during the initialization program. Any registers or main memory locations which are dedicated under a particular SUMC configuration must appear in appropriate EQUIVALENCE statements. These equivalence statements would require modification when changes in dedicated register assignments are made. The initialization operation for simulated SUMC main memory will of course include the input of the SUMC target program.

The simulation diagnostics which are available to the user - SNAP, TRACE, SPM DUMP, and MM DUMP - are controlled through a set of diagnostic

keys which trigger an appropriate printout at a specified point in the program. The diagnostics keys, if any, are specified by the user and input to the simulator by the INITLZ routine.

Finally, those simulation variables which are required internally by the simulator are initialized by INITLZ. Figure III-4 is a flow diagram showing the distinct operations performed during initialization by the INITLZ subroutine.

The first three operations performed by INITLZ, as shown in the flow diagram, are:

- dimension variables and define COMMON
- EQUIVALENCE statements
- initialize simulation variables.

These initialization operations require no input from the user, but are handled internally by the simulator. The final four operations require external inputs to the simulator and the nature of these inputs is described in the following paragraphs.

- a. READ user variables. The current version of the simulator allows the user to specify twelve of the key target computer parameters in the form of input data. Table III-5 lists the twelve variables which must be initialized by the user and Appendix I, SUMC Simulator User's Manual, specifies data formats to be followed for proper input.
- b. Initialize SPM registers. Part of the SPM initialization procedure is the specification of the function of SPM registers. This is done in part by the user as inidcated by Table III-5 and variables LOCG, LOCT, and LOCF. Armed with this information, along with appropriate DIMENSION statements for each block of registers, the exact location of each general register, floating point register, and temporary storage register is known to the program. The function and location of all other registers in scratch pad memory are specified for the program through EQUIVALENCE statements.
- c. READ diagnostics keys. Any of the available simulator diagnostics which the user may wish to exercise must be activated through

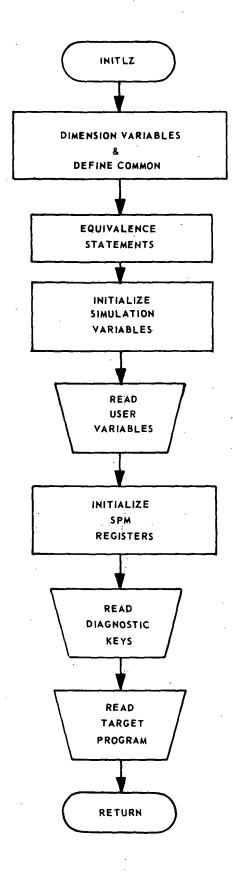


FIGURE III-4. FLOW DIAGRAM OF INITLZ ROUTINE

Table III-5. Target Computer Parameter Values Specified During Simulation

Variable	Parameter Description					
IHOST	Host computer word length					
ITARG	Target computer word length					
MAXCOR	Number of addressable locations in target MM					
LOBOUN	Target MM lower bound address					
JIBOUN	Target MM upper bound address					
MAXSPM	Number of registers in target SPM					
LOCG	Offset to first SPM general register					
LOCT	Offset to first SPM temporary register					
LOCF	Offset to first SPM floating-point register					
IFWA	Target program first word address					
INADDR	Target program first instruction address					
MAXTIM	Maximum simulated execution time					

the appropriate diagnostics input data. The INITLZ routine is presently designed to read this data from cards supplied by the user. A detailed description of the simulator diagnostics features is included in a later section of this report. The proper data formats as well as the deck set-up used for diagnostics input are given in Appendix I, SUMC Simulator User's Manual.

- d. READ target (SUMC) computer program. This portion of the INITLZ routine reads the target program which is to be simulated. The program is input in SUMC machine language form since the actual program input consists of the target SUMC main memory map. This memory map is stored in the IMAINM array, which will contain the simulated contents of target computer main memory throughout the simulation. The data formats and deck set-up for input of the target program are also given in Appendix I.
- 3. <u>Instruction Parse and Execute</u>. The nucleus of the SUMC interpretive simulator is made up of two subroutines which simulate the instruction fetch and execute operations. The first of these subroutines, FECHM, performs the following functions:
  - Validate instruction address
  - Fetch one-, two-, or three-halfword instruction from simulated SUMC main memory
  - Classify current instruction and parse contents accordingly
  - Validate all instruction operand addresses and fetch appropriate data.

The second subroutine, OPDEF, is called if FECHM is correctly executed and performs the following functions:

- Interpretively execute the instruction
- Validate simulated execution
- Place results in appropriate registers in target computer form
- Update timers and statistics variables.

The FECHM and OPDEF subroutines act in a supervisory capacity during the execution of each target instruction. That is, all basic operations required during the instruction execution phase are performed within the FECHM and OPDEF routines; however, frequently used or mundane arithmetic operations are processed by called subroutines or function subprograms. In addition, in the presence of error conditions or interrupts, control is transferred to an appropriate service subroutine.

A flow diagram of the basic FECHM subroutine is shown in Figure III-5. The diagram is simplified but nevertheless illustrates all basic operations and control functions executed by FECHM. An explanation will be given here of the basic steps followed in performing the simulated fetch operation.

- a. The initial action taken following a CALL to the FECHM subroutine is the validation of the current instruction address which is represented by the integer variable PCNTR. Two checks are made--the first test determines whether PCNTR is larger than the maximum number of addressable locations in simulated main memory and the second test determines whether PCNTR addresses a memory location which falls within the target program area of simulated main memory. If either of the tests fail, an error flag is set to identify the anomaly and an error termination routine, ERINS, is called.
- b. If PCNTR addresses a valid target program location, the instruction is fetched from IMAINM in halfword segments. Immediately after a fetch of the first halfword and the extraction of the instruction op code, a check is performed to determine (1) the validity of the op code and (2) the instruction classification. If the op code is invalid, the program is terminated by setting the appropriate error flag and calling ERINS. In the absence of any errors, the remaining one or two halfwords which make up the complete instruction are fetched from IMAINM (except in the case of an RR instruction which is comprised on only a single halfword). The number of helfwords making up a particular instruction is of course a function of the op code.

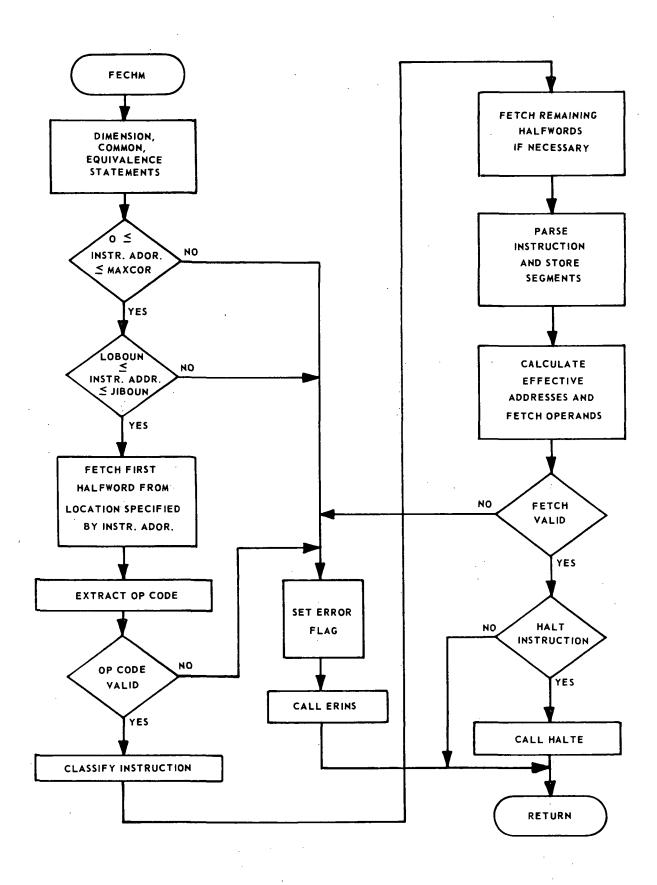


FIGURE 111-5. FLOW DIAGRAM OF FECHM ROUTINE.

- c. As each instruction halfword is fetched, the information contained in each segment of the halfword is parsed out and stored in a separate array, ISEGTA, which is used to store all components of the current instruction as FORTRAN variables. In addition, the effective addresses of any instruction memory operands are calculated and these operands, if any, are fetched from IMAINM and stored as FORTRAN variables.
- d. As the current instruction is fetched from IMAINM and parsed by the FECHM subroutine, each instruction operand or address is validated before proceeding further. If errors or interrupt conditions are detected, appropriate flags are set to identify the source and service subroutines are called. Unless a target program HALT instruction is being processed, control is relinquished to the MAINLIN supervisor routine immediately after the fetch is completely validated.

A flow diagram of the basic OPDEF subroutine is shown in Figure III-6. This subroutine will only be called following the successful completion of an instruction fetch and simulates the execution of the current target instruction. The basic steps followed during OPDEF execution are explained in the following paragraphs.

- a. After initializing the program constants which are needed by the OPDEF subroutine, a computed GO TO transfers control to that portion of the routine which will interpretively execute the fetched instruction. Since the operation to be performed by the current instruction is uniquely defined by the instruction op code, it is this parameter which is used as the transfer control variable.
- b. During the execution of an instruction, both intermediate and final results are checked to determine whether an error has occurred or an interrupt condition is present. In either case, the identifying flags will be set and the appropriate error termination or interrupt service routine will be called.
- c. Although the interpretive nature of the simulator allows the use of host computer hardware for efficient execution of each instruction, all instruction results must be stored in the proper simulated

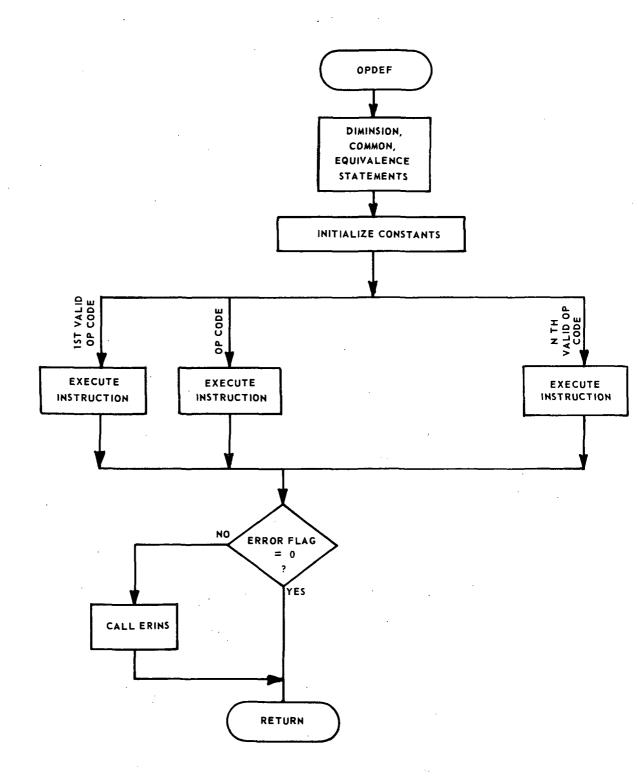


FIGURE III-6. FLOW DIAGRAM OF OPDEF

registers in exact SUMC target computer form at the conclusion of each instruction. That is, fidelity in yielding the correct result for an arbitrary instruction is the criterion rather than fieldity in executing the precise SUMC sequence to obtain the result. Furthermore, determination of the validity of a result occurs at the level of visibility to the programmer. This means that during the execution sequence, the simulator maintains the contents of computer storage that are available to the programmer but does not necessarily maintain registers, status indicators and other computer storage not available for reference by the programmer.

- d. Following the error-free execution of any instruction and a return to the MAINLIN supervisory routine, a CALL is issued to the TIMER subroutine in order to update simulation statistics. Figure III-7 shows the basic flow diagram for the TIMER routine and the following paragraphs give further details concerning statistics updating.
  - The program variable IOFFST is an instruction counter and is incremented by one following the successful execution of each target program instruction.
  - The complete set of all target computer instructions has been divided into ten distinct classes for statistics purposes. These classes are:
    - (1) Register-Register exclusive of other categories
    - (2) Arithmetic
    - (3) Logical
    - (4) Testing
    - (5) Branch
    - (6) Shift
    - (7) Input/Output
    - (8) Special
    - (9) Privileged
    - (10) Executive Call

A count of the number of target instructions of each class which have been executed is kept current during a simulation. The TIMER routine increments the appropriate class count by one following each instruction execution. The

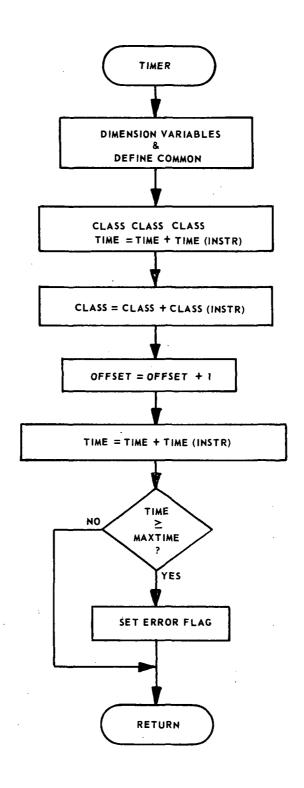


FIGURE III-7. FLOW DIAGRAM OF TIMER ROUTINE

total number of instructions processed in each class is available when the simulation is terminated.

- The total simulated execution time is also computed at the conclusion of each instruction execution. This total is computed by adding the time which would be required by the target computer for executing the current instruction to the accumulated time.
- In a similar manner, the simulated execution time associated with each of the instruction classes mentioned above is computed by TIMER. When the simulation is terminated, the total execution time attributed to each of the ten classes of instructions is available.

If the current simulated execution time computed by the TIMER subroutine is less than the allowable maximum execution time, the program executes a normal return to the MAINLIN routine. In this event, barring any pending interrupts, another simulation cycle begins with an instruction fetch. If the accumulated execution time exceeds the specified maximum time, an error flag is set and the program is terminated.

- 4. <u>User Diagnostic Aids</u>. The SUMC interpretive simulator includes five basic types of diagnostic routines which the user may take advantage of:
  - SNAPSHOTS of selected target main memory locations
  - TRACE of contents of key target registers
  - DUMP of contents of scratch pad memory
  - BLOCK DUMP of selected portion of target main memory
  - FULL DUMP of target main memory

To provide the necessary user control over the simulator diagnostics when operating on the IBM 7094 host computer, a group of diagnostics data cards must be included as part of the simulator input. These data cards are read by the program during the execution of the initialization routine, INITLZ, and serve to activate or deactivate each of the above diagnostic aids. When any of the diagnostic routines is activated,

supporting numerical data must also be included in the input data to provide control information which triggers the diagnostic execution at the desired time.

The simulator includes separate subroutines which perform diagnostics checking and processing following each simulated instruction execution. These routines are called by the primary control loop, MAINLIN, to collect any data requested by the user at that particular point in the program just prior to the execution of the current target instruction. The following sections will give a detailed explanation of each of the five diagnostics functions which are performed by the simulator.

- a. SNAP diagnostic. This diagnostic feature allows the user to obtain a printout of up to nine selected main memory locations at some predetermined point in the program. A CALL SNAPRD statement in the program initialization routine transfers simulator control to the subroutine, SNAPRD, which reads all SNAP information supplied by the user. A flow diagram of the SNAPRD subroutine is shown in Figure III-8. SNAPRD inputs data as follows:
- (1) READ SNAP. A single logical variable, SNAP, is read first and, if its value is true, additional SNAP data is sought. If its value is false, the user desires no SNAP diagnostics for the program under test and SNAPRD relinquishes control back to INITLZ.
- (2) READ FSNAP. This variable is given the value true if the user wishes to obtain a snapshot of specified main memory locations following each target instruction execution. Two additional data cards must be present when a full snap is specified—one card which specifies the number of MM locations to be snapped and the following lists the target memory addresses whose contents are to be printed. In addition, if a FULL SNAP has been requested, no other SNAP diagnostic may be present during the simulation. Therefore, control is transferred back to INITLZ after the FULL SNAP data has been read.
- (3) READ TISNAP. If a FULL SNAP has not been requested, other SNAP diagnostics are checked, beginning with the TIME-INTERVAL SNAP.

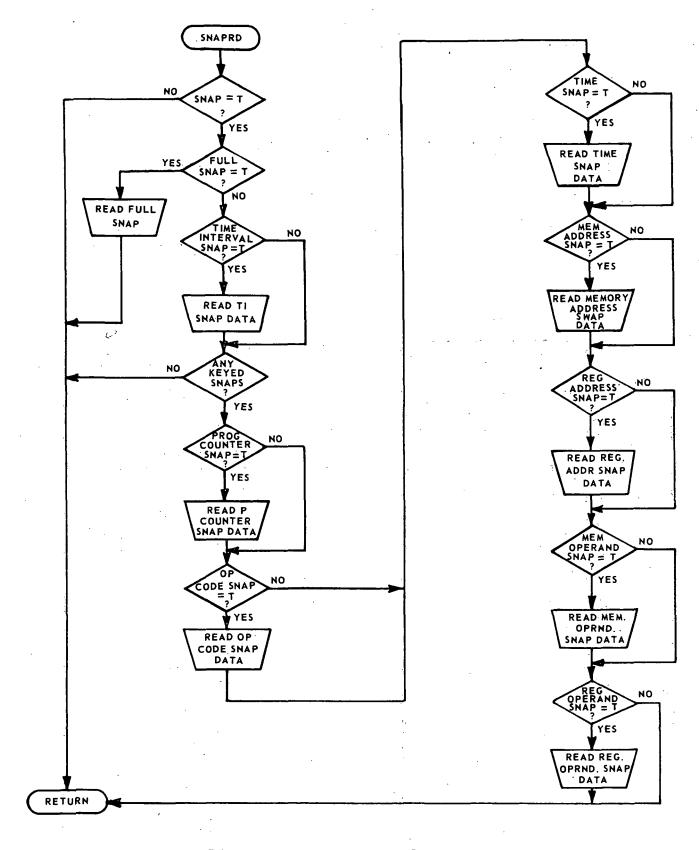


FIGURE III-8. FLOW DIAGRAM OF SNAPRD ROUTINE

For proper execution of this diagnostic, if activated, the user must specify the number of memory locations to be snapped and their addresses as well as the starting time for the SNAP execution, the time interval between each SNAP, and the time at which the final SNAP is to occur. For simplicity, only one time-interval SNAP routine may be requested for a particular simulation.

- (4) READ KSNAP. A single logical variable is read at this point to determine whether any keyed SNAP diagnostics are desired during program execution. If KSNAP=.FALSE., no keyed SNAP diagnostics are wanted and control is transferred back to INITLZ since only keyed SNAP data remains to be read by SNAPRD. If KSNAP-.TRUE., additional data cards must be read by SNAPRD which indicate the SNAP keys and corresponding memory locations to be printed.
- (5) READ PCSNAP. This is the first of seven keyed SNAP diagnostics which must be activated or deactivated whenever the previously mentioned KSNAP variable indicates the presence of one or more keyed SNAP requests. Whenever PCSNAP=.TRUE., a program-counter-keyed SNAP is desired by the user and data is read specifying the program counter values which act as triggers along with the corresponding memory locations whose contents are to be snapped. PCSNAP=.FALSE. indicates the absence of any program-counter-keyed SNAP requests or data pertaining to such.
- (6) READ OCSNAP. The OCSNAP logical variable indicates the presence or absence of an op-code-keyed SNAP request. If OCSNAP= .TRUE., an op-code-keyed SNAP diagnostic is wanted by the user and additional data is read specifying op code values which act as triggers and corresponding memory locations whose contents are to be snapped. OCSNAP=.FALSE. will of course require no additional data.
- (7) READ TSNAP. This logical variable indicates the presence/absence of any time-keyed SNAP requests. If TSNAP=.TRUE., one or more time-keyed SNAP diagnostics are wanted and additional data is read specifying at which simulated execution times the SNAP data is to be collected and also the memory locations whose contents are to be snapped.

- (8) READ MASNAP. The logical variable MASNAP indicates the presence/absence of any memory-address-keyed SNAP diagnostics. If MASNAP=.TRUE., memory-address-keyed SNAP diagnostics are wanted and appropriate data is read specifying the target memory locations to be snapped. MASNAP=.FALSE. requires no additional data.
- (9) READ RASNAP. The presence or absence of register-address-keyed SNAP diagnostics is indicated by the RASNAP variable. If RASNAP=.TRUE., data must be included giving the target instruction register address keys which trigger the SNAP and the memory locations to be snapped. No additional data is required when RASNAP=.FALSE.
- (10) READ MOSNAP. The logical variable MOSNAP indicates the presence/absence of memory-operand-keyed SNAP diagnostics. This diagnostic is identical to the memory-address-keyed SNAP with the exception that the contents of the specified memory address act to trigger the SNAP. Therefore, when MOSNAP=.TRUE., the octal contents of each memory address must also be included in the necessary data.
- (11) READ ROSNAP. The presence/absence of register-operand-keyed SNAP diagnostics is indicated by the logical variable ROSNAP. This diagnostic is identical to the register-address-keyed SNAP with the exception that the contents of the specified register address must be included in the necessary data when ROSNAP=.TRUE. and act to trigger the SNAP.

When any of the SNAP diagnostics discussed above are activated, two additional data values must be specified. First, for each set of memory locations which are to have their contents printed at SNAP execution time, the number of memory locations specified to be SNAPPED must be given. Second, the number of SNAP keys of each type, i.e., program-counter-keys, op-code-keys, etc., must be specified whenever a keyed SNAP diagnostic is activated.

Appendix I contains a detailed layout of the data cards which make up the SNAP diagnostics data deck. This layout gives a brief explanation of each data card which may be present as well as indicating proper card formats, proper card sequence, and data needed to activate any combination of the available SNAP diagnostics.

The SNAPEX subroutine is part of the primary simulator control loop, MAINLIN, and is called just prior to the execution of each target instruction. This routine is responsible for checking all SNAP diagnostic keys to determine whether a SNAP response is appropriate. If the user, by supplying the proper SNAP diagnostics data cards, has requested a SNAPSHOT of certain target main memory locations at this point in the program, this data is collected for printout by the SNAPEX routine before the pending target instruction is executed.

- b. TRACE diagnostic. This diagnostic feature makes it possible for the user to obtain a printout of the contents of key target computer registers at a predetermined point in the program. The user specifies the TRACE diagnostic keys, which serve to trigger the TRACE printout at the proper time, through a set of TRACE data cards that are read by the TRACRD subroutine. The TRACRD routine is called during program initialization and a flow diagram of this routine is shown in Figure III-9. TRACRD inputs data as follows:
- (1) READ TRACE. The first value which is read by the TRACRD routine is the logical variable TRACE, and if its value is logical .TRUE., additional TRACE data is sought. If TRACE=.FALSE., the user desires no TRACE diagnostics for the program and TRACRD relinquishes control to INITLZ.
- (2) READ FTRACE. If the logical variable FTRACE=.TRUE., the user will obtain a trace of the contents of all key target computer registers following each target instruction execution. If this FULL TRACE is activated, no other TRACE diagnostics can be specified since their presence would simply yield redundant TRACE information. Only when FTRACE=.FALSE. does the routine search for other TRACE diagnostic data.
- (3) READ TITRAC. A time-interval TRACE is requested through the logical variable TITRAC. This diagnostic yields a TRACE of the key target computer registers at a specified time interval beginning and

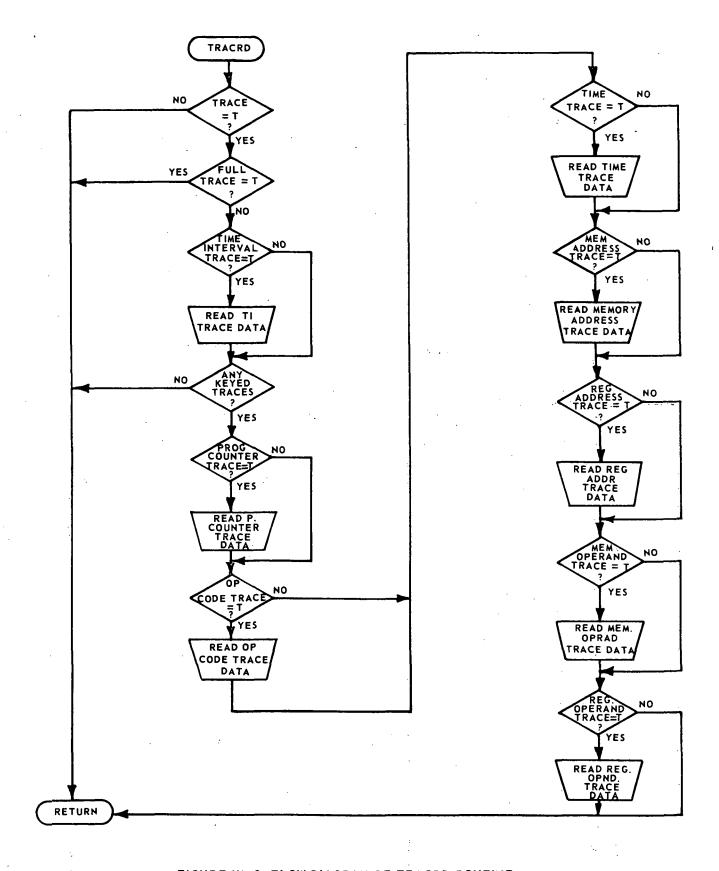


FIGURE III-9. FLOW DIAGRAM OF TRACRD ROUTINE

ending at those times specified by the user. If TITRAC=.TRUE., an additional data card must be present to supply TRACE start time, stop time, and time interval.

- (4) READ KTRACE. A single logical variable is read at this point to determine whether any keyed TRACE diagnostics are desired during program execution. If KTRACE=.FALSE., no keyed TRACE diagnostics are wanted and control is transferred back to INITLZ since only keyed TRACE data remains to be read by TRACRD. If KTRACE=.TRUE., additional data cards, as discussed below, are read by TRACRD in order to input all TRACE keys.
- diagnostics which must be activated or deactivated whenever the previously mentioned KTRACE variable indicates the presence of one or more keyed TRACE requests. Whenever PCTRAC=.TRUE., a program-counter-keyed TRACE is desired by the user and data is read specifying the program counter values which are to act as triggers along with the number of consecutive instructions which are to be traced. PCSNAP=.FALSE. indicates the absence of any program-counter-keyed TRACE requests or data pertaining to such.
- (6) READ OCTRAC. The OCTRAC logical variable indicates the presence or absence of an op-code-keyed TRACE request. If OCTRAC=.TRUE., an op-code-keyed TRACE diagnostic is wanted by the user and additional data is read specifying op code values which act as triggers and the corresponding number of instructions to be traced. OCTRAC=.FALSE. of course requires no additional data.
- (7) READ TTRACE. This logical variable indicates the presence/absence of any time-keyed TRACE requests. If TTRACE=.TRUE., one or more time-keyed TRACE diagnostics are wanted and additional data specifies at which simulated execution times the TRACE data is to be collected and also the number of instructions for which each TRACE is to be in effect.
- (8) READ MATRAC. The logical variable MATRAC indicates the presence/absence of any memory-address-keyed TRACE diagnostics. If

MATRAC=.TRUE., memory-address-keyed TRACE diagnostics are wanted and appropriate data is read specifying the target instruction memory addresses which trigger the TRACE output and the number of instructions to be traced. MATRAC=.FALSE. requires no additional data.

- (9) READ RATRAC. The presence or absence of register-address-keyed TRACE diagnostics is indicated by the RATRAC variable. If RATRAC=.TRUE., data must be included giving the target instruction register address keys which trigger the TRACE and the corresponding number of instructions to be traced. No additional data is required when RATRAC=.FALSE..
- (10) READ MOTRAC. The logical variable MOTRAC indicates the presence/absence of memory-operand-keyed TRACE diagnostics. This diagnostic is identical to the memory-address-keyed TRACE with the exception that the contents of the specified target instruction memory address act to trigger the TRACE. Therefore, when MOTRAC=.TRUE., each TRACE key includes a target memory address, its corresponding contents, and the number of instructions to be traced.
- (11) READ ROTRAC. The presence/absence of register-operand-keyed TRACE diagnostics is indicated by the logical variable ROTRAC. This diagnostic is identical to the register-address-keyed TRACE with the exception that the contents of the specified register address must be included in the necessary data when ROTRAC=.TRUE. and act to trigger the TRACE.

Appendix I contains a detailed layout of the data cards which make up the TRACE diagnostics data deck. This layout gives a brief explanation of each data card which may be present as well as indicating proper card formats, proper card sequence, and data needed to activate any combination of the available TRACE diagnostics.

The TRACEX subroutine is called by the simulator primary control loop, MAINLIN, just prior to the execution of each target instruction. This routine is responsible for checking TRACE diagnostics keys (if any) to determine whether a register TRACE is appropriate. If the user, by supplying the proper TRACE diagnostics data cards, has requested a TRACE

of the key target computer registers at this point in the program, this data is collected for subsequent printout by the TRACEX routine before the pending target instruction is processed.

- c. SPM DUMP Diagnostic. This diagnostic feature enables the user to obtain a dump of the contents of SUMC scratch-pad-memory at a predetermined point in the program. The user must specify the SPM DUMP keys, which serve to trigger the dump at the proper time, through a set of SPM DUMP data cards that are read by the SPMDRD subroutine. The SPMRRD subroutine is called during program initialization and a flow diagram of this routine is shown in Figure III-10. SPMDRD inputs data as follows:
- (1) READ SPMD. The first value which is read by the SPMDRD routine is the logical variable SPMD, and if its value is logical .TRUE., additional SPM DUMP data is sought. If SPMD=.FALSE., the user does not want a SPM DUMP at any point during the simulation and SPMDRD does not search for additional data but relinquishes control to INITLZ.
- DUMP diagnostics which must be activated or deactivated whenever the previously mentioned SPMD variable indicated the presence of one or more keyed SPM DUMP requests. Whenever PCSPMD=.TRUE., a program-counter-keyed SPM DUMP is desired by the user and two additional data cards must be read. The first card specifies the number of dump keys to be entered as input and the second gives the values of the program counter keys which act as triggers for SPM DUMP execution. PCSPMD=.FALSE. indicates the absence of any program-counter-keyed SPM DUMP requests or data pertaining to such.
- (3) READ OCSPMD. The OCSPMD logical variable indicates the presence or absence of any op-code-keyed SPM DUMP requests. If OCSPMD=.TRUE., an op-code-keyed SPM DUMP diagnostic is wanted by the user and two additional data cards specify (a) number of op code keys to be entered an input and (b) values of the op code keys which act as SPM DUMP triggers. OCSPMD=.FALSE. of course requires no additional data.

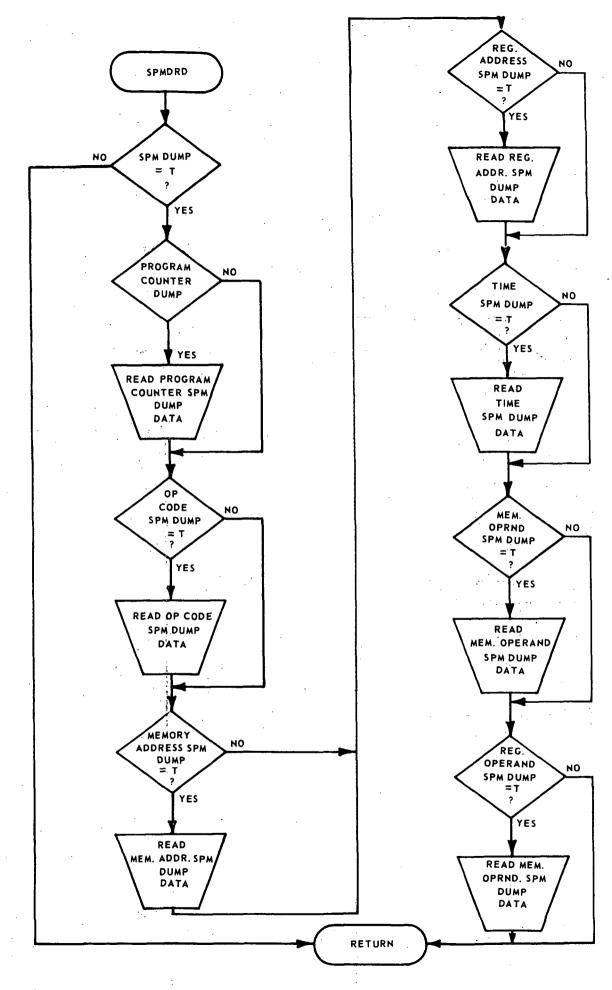


FIGURE III-10. FLOW DIAGRAM OF SPMDRD ROUTINE

- (4) READ MASPMD. The logical variable MASPMD indicates the presence/absence of any memory-address-keyed SPM DUMP diagnostics. If MASPMD=.TRUE., memory-address-keyed SPM DUMP diagnostics are wanted and two additional data cards specify (a) number of memory address keys to be entered and (b) instruction memory addresses which will act as keys to trigger a SPM DUMP. MASPMD=.FALSE. requires no additional data.
- (5) READ RASPMD. The presence or absence of register-address-keyed SPM DUMP diagnostics is indicated by the RASPMD variable. If RASPMD=.TRUE., one or more register-address-keyed SPM DUMP requests are present and two additional data cards specify (a) number of register address keys to be entered and (b) instruction register addresses which will act as keys to trigger a SPM DUMP. RASPMD=.FALSE. requires no additional data cards.
- (6) READ TSPMD. This logical variable declares the presence/absence of time-keyed SPM DUMP diagnostic requests. If TSPMD=.TRUE., time-keyed SPM DUMP diagnostics are wanted by the user and additional data includes (a) number of time keys to be entered and (b) simulated elapsed time at which each SPM DUMP is to be executed.
- (7) READ MOSPMD. The logical variable MOSPMD indicates the presence/absence of any memory-operand-keyed SPM DUMP diagnostics. If MOSPMD=.TRUE., SPM DUMP diagnostics which are keyed by instruction memory operands are wanted by the user and two additional data cards supply (a) number of memory operand keys to be entered and (b) the instruction memory addresses and their corresponding contents which will act as keys to trigger the desired SPM DUMP executions.
- (8) READ ROSPMD. The logical variable ROSPMD indicates the presence/absence of register-operand-keyed SPM DUMP diagnostics. If ROSPMD=.TRUE., SPM DUMP diagnostics are wanted which are keyed by instruction register operands and two additional data cards specify (a) number of register operand keys to be entered and (b) the instruction register addresses and their corresponding contents which will act as keys to trigger SPM DUMP diagnostics.

A detailed layout of the data cards which comprise the SPM DUMP diagnostics data deck is contained in Appendix I. This layout provides a brief description of each data card which may be present as well as indicating proper card formats, proper card sequence, and data needed to activate any combination of the available SPM DUMP diagnostics.

The SPMDEX subroutine is called by the simulator primary control loop, MAINLIN, just prior to the execution of each target instruction. This routine checks all SPM DUMP diagnostics keys to determine whether a dump of SPM registers is wanted by the user at this point in the program. Whenever a SPM DUMP is appropriate, the data is collected by SPMDEX before the pending target instruction is processed.

d. Block MM Dump Diagnostic. This simulator diagnostic allows the user to obtain a dump of a selected block of contiguous target computer main memory locations at some predetermined point in the program. The user must specify the program counter values which will act to trigger the block MM DUMP at the desired point in the program. All diagnostics data which is needed to control block MM DUMP operations is read by the MMDRD subroutine. This routine is called during program initialization and the flow diagram is shown in Figure III-11.

The first value which is read by the MMDRD routine is the logical variable BLMMD, and if the logical value is .TRUE., additional block MM DUMP data is sought. If BLMMD=.FALSE., the user desires no block MM DUMP diagnostics and further supporting data should not be present.

The supporting data which is required when BLMMD=.TRUE. consists of (a) a single data card which specifies the number of program counter DUMP keys to be entered and (b) a set of data cards (one for each program counter key), each of which contains the program counter value, the block MM DUMP start address, and the number of target main memory locations to be dumped.

Appendix I contains a detailed layout of the data cards which comprise the block MM DUMP diagnostics data deck. The layout provides a brief description of each data card which may be present as well as indicating proper card formats and card sequence.

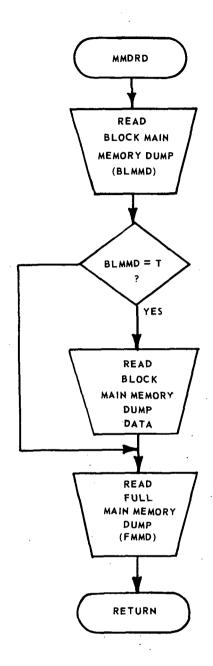


FIGURE III-11. FLOW DIAGRAM OF MMDRD ROUTINE

The execution of a block MM DUMP during simulation of a target program is accomplished by the BLMDEX subroutine. This routine is called by the simulator primary control loop, MAINLIN, just prior to the execution of each target instruction. BLMDEX compares each of the program counter DUMP keys with the current simulated target program counter, and if a match is found, the appropriate data is collected for subsequent printout.

- e. Full MM DUMP Diagnostic. The user may obtain a full DUMP of the contents of all target computer main memory locations at the termination of a target program simulation. A full MM DUMP is available only at program termination and is requested by the user through a single data card which is read by the previously mentioned MMDRD routine. As shown in Figure III-11, the MMDRD subroutine reads the logical variable FMMD before returning to INITLZ. If FMMD=.TRUE., a full target MM DUMP is performed at program termination. The value of the FMMD variable is supplied by the user as the last data card in the diagnostics data deck, as shown in the data card layouts of Appendix I.
- f. Diagnostics Header Information. All of the diagnostic features which have been discussed supply the user with information concerning the contents of certain target computer (SPM or MM) registers at a particular point in the simulation of a target program. In order to identify the exact point during target program execution that a particular diagnostics output was obtained, a block of header information forms the preamble to all diagnostics printouts. The information supplied by each header block includes:
  - type of diagnostic in effect
  - number of instructions executed
  - simulated elapsed time
  - current instruction address
  - current instruction contents
  - instruction register operands
  - instruction memory operands.

- 5. Program Termination. When a particular SUMC program simulation is terminated, it may be due to any one of a number of different possible causes. The cause of the program termination will have a direct bearing on simulator response and the data which is provided at the conclusion of a program. Whenever possible, the termination cause is identified and a table of program statistics is provided to the user. The following paragraphs will discuss the different simulation conditions which lead to program termination and simulator response for each condition.
- a. Invalid Simulation Definition. This error condition results whenever data which is supplied by the user for simulation initialization and control is invalid. The user must supply three types of definition data:
  - SUMC target computer architectural parameters
  - SUMC register initialization data
  - diagnostics data

In the first two cases, erroneous data will not prevent the simulator from beginning target program execution; however, it is not predictable at what point during the simulation this input error will be detected. When detected, it will be identified as a program interruption and the appropriate interrupt response will be taken. In the third case, the host computer input operations will be affected and termination action will depend only on host computer characteristics.

- b. Error Interrupts. Two classes of interrupt conditions are considered to be error conditions and will lead to program termination. These are
  - Program interruption and
  - Machine-check interruption.

A complete discussion of the SUMC interrupt scheme which includes the above two conditions as well as three additional interrupt conditions is given in the next section, <u>Simulator Interrupt Capability</u>.

Whenever either of the error interrupt conditions occurs, appropriate interrupt servicing routines are called by the simulator and upon

their completion, the program is terminated. The information supplied to the user at termination includes an error flag identifying the cause and a table of simulation statistics. The error flag is set as follows:

Error Flag	Meaning				
1	Operation exception interrupt				
2	Privileged-operation exception interrupt				
3	Execute exception interrupt				
4	Addressing exception interrupt				
5	Specification exception interrupt				
6	Data exception interrupt				
7	Fixed-point-overflow exception interrupt				
8	Fixed-point-divide exception interrupt				
9	Exponent-overflow exception interrupt				
10	Exponent-underflow exception interrupt				
11	Significance exception interrupt				
12	Floating-point-divide exception interrupt				
13	Machine-check interrupt				
14	Memory boundary violation				
15	Time overflow				
16	Wait state				

The simulation statistics include information concerning each of the ten classes of instructions previously discussed in Section III-B.3. For termination due to an error interrupt, the following information is made available:

- number of instructions of each class which were executed
- amount of time used in executing each class of instruction
- percentage of total simulated elapsed time used in executing each class of instruction
- total number of instructions executed
- total simulated elapsed time

- c. Simulation Errors. In addition to detecting those error conditions which lead to a target computer interrupt response, the simulator checks two additional error conditions which also result in program termination. These are:
  - target computer memory boundary violation
  - simulated elapsed time overflow

A boundary violation will occur whenever instructions or data is addressed by the target program and this address exceeds the target computer core size. A time overflow occurs when the simulated elapsed time exceeds the maximum program execution time specified by the user prior to beginning the simulation. When either of these errors is detected during a simulation, the program is terminated immediately. A printout of the error flag value identifies the termination cause for the user and the normal statistics information is also printed following this type of program termination.

- d. Wait State. If the SUMC simulator executes an instruction which places the target machine in the WAIT state, the simulation response will be identical to that obtained due to normal target program completion. The single exception is that an error flag is printed indicating the WAIT state.
- e. Target Program Completion. A normal termination of the simulator program occurs when all target program instructions have been executed in an error-free fashion. Unless the user has requested specific diagnostics, the only information necessary at the time of a normal program completion will be the usual statistics table.

The present version of the SUMC simulator does not possess a restart capability although provisions have been made to add this feature at a later date. This feature will of course have its greatest impact on the program termination portions of the simulator. Future restart capabilities will be discussed in detail in a later section which deals with possible simulator enhancements.

6. SUMC Simulator Interrupt Capability. The SUMC computer which presently acts as the target machine for the current version of the simulator has an interrupt scheme modeled after that of the IBM 360 system. Under this setup, five classes of interrupt conditions are present, which are input/output, program, supervisor-call, external, and machine check interruptions.

An interruption consists of storing the current Program Status Word (PSW) as an old PSW and fetching a new PSW. Interruptions are taken only when the CPU is interruptible for the interruption source. The system mask can be used to mask I/O and external interruptions; the program mask can be used to mask three of the twelve program interruptions; and the machine-check mask can be used to mask machine-check interruptions.

The simulator checks for interruptions after one instruction interpretation is finished and before a new instruction interpretation is started. This check is performed within the primary control loop each time the simulator returns from an interpretive instruction execution. The action taken by the simulator upon the detection of an interrupt condition is as follows:

- When any type of interrupt is detected, the INTRPS subroutine is called for the purpose of maintaining the stack of pending interrupts. The current interrupt is added to the stack according to its predetermined servicing priority. The INTRPS subroutine is also responsible for maintaining the interrupt stack whenever it is modified due to a pending interrupt being "pulled" for servicing.
- The IMMPSW routine is called to convert the current PSW to an old PSW format and store this PSW in the appropriate main storage location.
- The ISPPSW routine is called to convert the new PSW in main storage into the current PSW format and store this PSW in simulated scratch pad memory.

- When an interruption is detected, the instruction which is currently being executed may or may not be completed depending on the type of interruption. Furthermore, interruptions caused by error conditions will result in a call of the ERINS subroutine which identifies the anomaly to the user and subsequently terminates the simulation program.
- If the interruption is not due to an error condition, an interrupt service routine, INTSER, is called which informs the user that the interrupt has occurred, before beginning the execution of the next instruction. The INTSER routine will eventually be expanded to perform all simulated interrupt servicing operations according to the interruption action of the simulation target computer. The present version of the SUMC simulation program simulates only interrupt detection and stack operations.

A summary of the target computer interruption conditions which must be checked by the simulator are given in Table III-6. This table lists, for each interruption source, the interruption code, system mask bits, interruption-length code, operation execution and simulation execution.

As discussed above, the present version of the interpretive simulator models the target SUMC interrupt detection and stacking operations but does not simulate the actual interrupt servicing operations. The interrupt servicing routines are highly dependent on the particular target computer being simulated and their implementation is planned for a later date, as outlined in the next section covering future simulator enhancements.

7. <u>Simulator Utility Routines and Functions</u>. There are a number of subroutines included in the simulation program which perform generic operations and which are used by different simulator modules. The following paragraphs give brief descriptions of these utility routines along with an explanation of their function.

Table III-6. SUMC Interruption Conditions

Source Identification	Interruption Code PSW Bits 16-31	Mask Bits	ILC Set	Operation Execution	Simulation Execution			
INPUT/OUTPUT (OLD PSW 56, NEW PSW 120, PRIORITY 4)								
Channel 1	00000001 aaaaaaa	0	x	completed	continued			
PROGRAM (OLD PSW 40, NEW PSW 104, PRIORITY 2)								
Operation Privileged Oper. Execute Addressing Specification Data Fixed-point ovfl. Fixed-point div. Exponent ovfl. Exponent unfl. Significance Floating-point div.	00000000 00000001 00000000 00000010 00000000	36 38 39	1,2,3 1,2 2 0,1,2,3 1,2 1,2 1,2 1,2 1,2 1,2 1,2 1,2	suppressed suppressed suppressed suppressed terminated completed suppressed completed completed suppressed	terminated			
SUPERVISOR-CALL (OLD PSW 32, NEW PSW 96, PRIORITY 2)								
Instruction bits	00000000 rrrrrrr		í	completed	continued			
EXTERNAL (OLD PSW 24, NEW PSW 88, PRIORITY 3)								
Interrupt key	00000000 nlnnnnn	7	х	completed	terminated			
MACHINE CHECK (OLD PSW 48, NEW PSW 112, PRIORITY 1)								
Machine malfunction	ccccccc ccccccc	13	х	terminated	terminated			

NOTES .

a = device address bits

 $r = bits of R_1, R_2 field of SVC instruction$ 

n = other external-interruption conditions

c = target computer-dependent bits

x = unpredictable

IAND(I,J) is a function subprogram which logically AND's the contents of the two locations specified by the arguments of the function and returns this result to the calling subprogram.

IOR(I,J) is a function subprogram which logically OR's the contents of the two locations specified by the arguments of the function and returns the result to the calling subprogram.

IER(I,J) is a function subprogram which performs the logical EXCLUSIVE OR of the contents of the locations specified by the arguments of the function and returns this result to the calling subprogram.

INTNOT(K) is a function subprogram which complements the contents of the location specified by the argument and returns this result to the calling subprogram.

ITWTSM(I) is a function subprogram which converts the two's-complement value of the argument to signed-magnitude representation and returns this result to the calling subprogram.

ISMTWO(I) is a function subprogram which converts the signed-magnitude value of the argument to two's-complement representation and returns this result to the calling subprogram.

ILOAD(SOURCE, SB, NB) is a function subprogram which will move a field of data from the source word and will right-justify it as the output argument. The remaining part of the output argument word will be filled with zeros.

ISTORE(SRC1,SRC2,SB,NB) is a function subprogram which will move a right-justified field of data of NB bits in length from SRC1 and will scale to position SB. This field will then replace the same scaled field portion of word SRC2. The word then formed becomes the output argument and is returned to the calling subprogram.

JEXBIN(IBUF, IST, ILNG) is a function subprogram which converts a hexadecimal character string to a binary representation. The conversion result is the binary equivalent of the ILNG hexadecimal characters beginning with character IST of the string IBUF. I2T1(I) and IIT2(I) are one's-complement: two's-complement conversion routines which will be implemented for later versions of the simulator. Present operation on the IBM 7094 host system, a signed-magnitude arithmetic machine, does not require the use of these routines.

ICOMP1(SOURCE,SB,NB) is a function subprogram which will complement a field of data in the source word. The NB bits beginning at bit position SB of the source word are one's-complemented in the output argument.

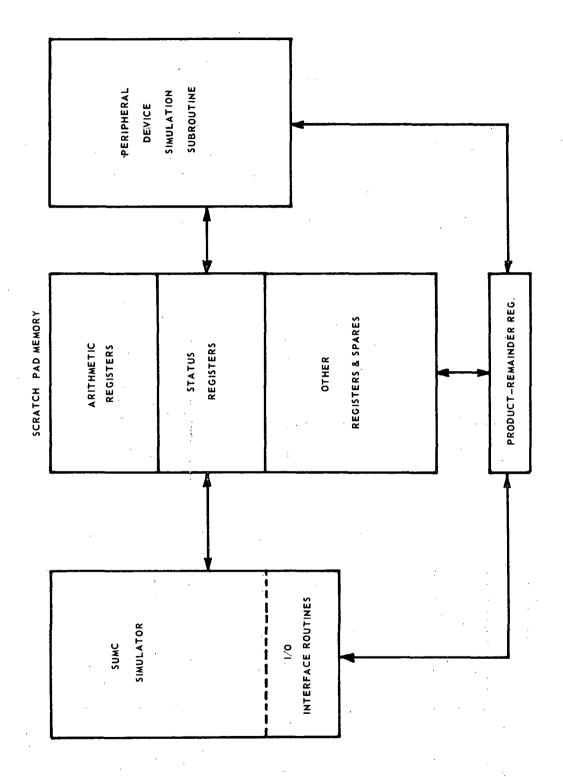
## C. Recommended Expansion and Enhancements

1. Input/Output Simulation. The present version of the SUMC interpretive simulator does not perform simulated I/O operations. The I/O processing characteristics of the SUMC target computer will vary greatly from one target machine to the next and, for this reason, an I/O simulation program package would not be appropriate for the basic SUMC simulation program. What would be appropriate, however, is a general purpose I/O interface routine which would form part of the basic simulator. This interface routine would coordinate I/O simulation operations between the basic simulator program and various peripheral device simulation subroutines which would be needed for a particular application.

Figure III-12 contains a diagram which indicates the communication paths which would be necessary for an I/O simulation scheme as discussed above. Under this setup, the SUMC simulator would maintain status information in the COMMON scratch pad memory array and also place and retrieve data in the product-remainder register (PRR) location. The peripheral device simulation routines would handle all I/O data transfers through the PRR while under control of the SPM status registers.

I/O simulation procedures will depend heavily on the particular application; however, an I/O interface routine for the SUMC simulator will perform at least the following functions:

Set/Reset appropriate status registers



- Place/Retrieve data in the PRR
- Issue CALL's to specified peripheral device simulation routines.

Peripheral device simulated elapsed time will be maintained by each device simulation routine and I/O task completion must signal a RETURN to the primary control loop of the SUMC simulator. All I/O processing routines are of course triggered by I/O interruptions of the target computer CPU.

- 2. <u>Simulator Execution Efficiency</u>. The SUMC instruction simulator has been designed with generality in mind as a key simulation objective. It is meant to be a basic, general-purpose simulator in two respects:
  - The simulator must have the capability to model a family of SUMC target machines, i.e., this computer family is expected to consist of machines with architectures and design parameters which may vary with the envisioned application.
  - The simulator must be easily transferrable between different host computers, i.e., the SUMC simulator development is being done using an IBM 7094 host system with plans for production runs on a Univac 1108 system. (In addition, it is expected that the simulator should be easily modified to eventually operate on several other large-scale commercial host systems.)

The desired generality of simulator design cannot be realized without paying the penalty of decreased execution efficiency. This inherent
design tradeoff on generality and efficiency can only be resolved through
carefully defined simulation objectives and continuing studies of the
basic simulator's execution efficiency. These studies are planned
following the initial simulator implementation and programming changes
will be made accordingly.

If the price to achieve a general-purpose simulator has been too great, there are several areas which may be investigated for

enhancement of simulator execution efficiency. These are:

- Rewriting any existing program code which has not already been written in the most efficient form.
- Converting basic subroutines from the standard FORTRAN IV source language to a more efficient machine language code whenever this will enhance execution speed.
- Employing host machine hardware to the maximum possible extent.
- Sacrificing any target computer generalities which are not explicitly desired.
- Employing the capabilities of the simulator supervisory
   I/O routines in lieu of the present FORTRAN I/O operations.
- 3. Target Instruction Set. The instruction set which has been implemented for the current SUMC target computer parallels that of the IBM 360 system. The present version of the SUMC simulator executes a selected subset of this set of machine instructions. If desired, the SUMC simulator could be expanded to execute the complete instruction set used by the IBM 360 system. This would basically require the addition of floating-point, I/O, and decimal arithmetic instructions to the present simulator. Table III-7 shows a complete list of all IBM 360 instructions and those which have been included in the present version of the simulator are marked.

One of the key enhancements presently planned for the interpretive simulator is the addition of a complete set of floating-point instructions and decimal arithmetic instructions. It is of course the ultimate aim of the interpretive simulator to be capable of processing the complete instruction set of the SUMC computer which at a particular time is serving as the simulation target computer.

4. <u>Interrupt Servicing Simulation</u>. As discussed previously in this report, the SUMC simulator has the present capability to model the target computer interrupt detection and stacking operations. The simulation of actual interruption servicing operations has not been a part

Table III-7. Instruction Implementation Status

04		Status	Code	Mnemonic	Status	Code	Mnemonic	Status
•	SPM	Х	40	STH	Х	80	SSM	х
05	BALR	х	41	LA	Х	82	LPSW	X
06	BCTR	х	42	STC	x	83		
07	BCR	x	43	IC	x	84	WRD	1
08	SSK		44	EX		85	RDD	1
09	ISK		45	BAL	x	86	BXH	x
0A	SVC	Х	46	BCT	Х	87	BXLE	х
10	LPR	X	47	BC	X	88	SRL	X
11	LNR	X	48	LH	х	89	SLL	Х
12	LTR	X	49	CH	X	8A	SRA	X
13	LCR	X	4A	AH	X	8B	SLA	X
14	NR	X	4B	SH	X	8C	SRDL	X
15	CLR	X	4C	MH	X	80	SLDL	X
		X	4E	CVD	^	8E	SRDA	X
16	OR VD	X	4E 4F	CVB		8F	SLDA	x
17	XR				.	90		X
18	LR	X	50	ST	X		STM	X
19	CR	X	54	N	X	91	TM	
1A	AR	X	55	CL	X	92	MVI	X
1B	SR	X	56	0	X	93	TS	X
1C	MR	X	57	X	X	94	NI	X
1D	DR	Х	58	L	X	95	CLI	X
1E	ALR	Х	59	C	X	96	OI	X
1F	SLR	Х	5A	A	X	97	XI	X
20	LPDR		5B	S	X	98	LM	X
21	LNDR	1	5C	M	X	9C	SIO	
22	LTDR		5D	D	X	9D	TIO	
23	LCDR		5E	AL	X	9E	н10	
24	HDR		5F	SL	X	9 <b>F</b>	TCH	
28	LDR		60	STD	1 1	D1	MVN	
29	CDR		68	LD	1	D2	MVC	Х
2A	ADR		69	CD	1	D3	MVZ	
2B	SDR	1	6A	AD	1 1	D4	NO	1
2C	MDR		6B	SD		D5	CLC	
2D	DDR	<b>!</b>	6C	MD	, ,	D6	oc	
2E	AWR	1	6D	DD .	1 1	D7	XC	1
2F	SWR		6E	AW	1	DC	TR	
30	LPER	[ ]	6 <b>F</b>	SW	1 4	DD	TRT	
31	LNER		70	STE	1 . 1	DE	ED	
32	LTER	}	78	LE	1	DF	EDMK	
33	LCER	<u> </u>	79	CE		F1	MVO	
34	HER	1 1	7A	AE	1	F2	PACK	1
38	LER	]	7B	SE		F3	UNPK	
39	CER	[ ]	7C	ME	1 1	F8	ZAP	
3A	AER	1	7D	DE	1	F9	CP	1
3B	SER	, ,	7E	AU		FA	AP	
3C	MER	}	7F	នប	1	FB	SP	
3D	DER	]	1	1	}	FC	MP	1
3E	AUR	,				FD	DP	1
3F	SUR		1			1		İ

X = Have been implemented for SUMC simulator.

of the present project. For simulator completeness, however, the simulation of the total interrupt response operations performed by the target computer is an essential part of future simulator enhancement studies.

The present SUMC target computer recognizes 16 different interruption conditions and future enhancement plans therefore include the implementation of at least this set of interrupt service routines. These interruptions are listed below.

- Program Interruptions
  - operation exception
  - privileged-operation exception
  - execute exception
  - addressing exception
  - specification exception
  - data exception
  - fixed-point overflow exception
  - fixed-point divide exception
  - exponent overflow exception
  - exponent underflow exception
  - significance exception
  - floating-point divide exception
- Supervisor-Call (SVC) Interruption
- Input/Output Interruptions
  - single I/O channel
- External Interruptions
  - interrupt key signals
- Machine-Check Interruption

#### SECTION IV. SUMMARY

The SUMC simulator has been designed to interpretively execute the instruction set of a SUMC target computer. Flexibility has been designed into the simulator so that a SUMC family of target computers may be simulated. This done by introducing simulation parameters which define the key architectural features of the target computer under consideration. The simulator is given added relevance to many users through a design objective requiring host machine independence for the simulator to the fullest possible extent. This goal is accomplished by isolating all host machine dependent functions performed by the simulator to a minimum number of distinct program modules.

After a brief description of the SUMC architecture and instruction set, a complete description of the SUMC interpretive simulator is given in Section III. In this section, following a discussion of simulator design principles, the different functional program modules making up the simulator are discussed separately. The simulator modules have been grouped under the following headings:

- primary control loop
- initialization
- instruction parse and execute
- diagnostics
- program termination
- program interruptions
- utility routines and functions

To supplement the simulator description given in Section III, the appendices found at the end of this report include:

- User's Manual to provide information for efficient use of the simulator covering deck setup, required data inputs, and data card formats;
- Module Descriptions to provide brief descriptions of all functional modules which comprise the complete simulator;

- SUMC Instructions to provide brief descriptions of the Breadboard System instructions which have been implemented in the interpretive simulator.
- Simulator Source Program Listing to provide a complete record of the SUMC simulator as it presently exists.
- Sample Output Listing to provide an example of the type of simulation output obtained when simulating a typical SUMC target program.

Recommended expansion and enhancements for the simulator are also pointed out in Section III. The following categories are covered:

- Input/Output
- Execution efficiency
- Target instruction set
- Interrupt servicing

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#### APPENDIX I. USER MANUAL

The intention of this section is to provide a brief but exact summary of the operational characteristics of the SUMC interpretive simulator program. Proper deck setup is illustrated for execution on the IBM 7094 host computer and detailed descriptions of all required or optional data cards is also given.

## A. Deck Setup

Figure A1-1 shows the basic components which make up the complete simulator source deck. The simulator is presently a self-contained set of program modules designed to operate in the batch programming mode. The following component decks are therefore required for execution of a SUMC program using the interpretive simulator.

- 1. <u>Host Control Cards</u>. This is a standard deck of control cards used by the host computer for processing a particular simulation job. The makeup of this set of cards is entirely dependent on the particular computer installation which is used as the host system.
- 2. <u>Simulator Modules</u>. This set of program modules comprises the basic SUMC interpretive simulator. The simulator has been modularized in this fashion for ease of implementation, convenience of program changes, and also to isolate host computer programming dependencies. A brief description of each program module included in the basic simulator is given in Appendix II.
- 3. <u>\$DATA Card</u>. This card is required under the IBM 7094 host system in order to signal the presence of user-supplied input data cards.
- 4. <u>Diagnostics Data</u>. This set of data cards provides the diagnostics keys and accompanying information needed to activate and execute any SNAP, TRACE, SPM DUMP, or MM DUMP diagnostics wanted by the user. A detailed explanation of the contents of this data deck is given later in this section.

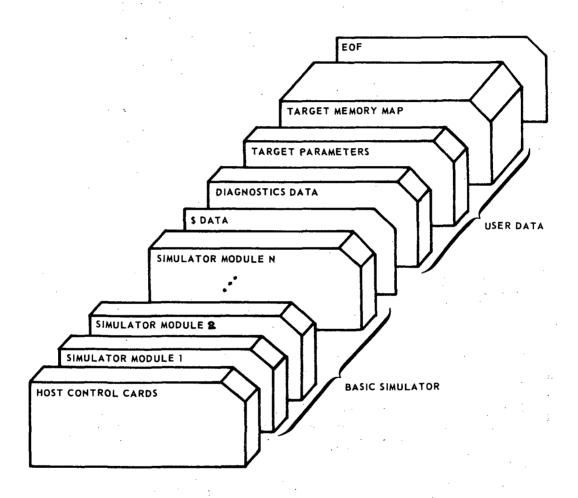


FIGURE A1-1. SUMC INTERPRETIVE SIMULATOR SOURCE DECK SETUP.

- 5. <u>Target Parameters</u>. The architectural features of the SUMC target computer which may be varied for a particular application are supplied with values appearing in this data deck. A detailed explanation of the data cards needed to assign values to the different parameters is given later in this section.
- 6. Target Memory Map. The target program which is to be interpretively executed by the SUMC simulator is described through data contained in the target memory map deck. Each card included in this deck contains a SUMC main memory address and the hexadecimal value which is to be loaded into the location. A detailed layout of this card deck will be given later in this section.

## B. Diagnostics Data Deck Setup

The following five pages present a detailed layout of the data cards which may be included in the user's diagnostics deck. The exact sequence required for input of this data as well as the necessary formats are given. The diagnostics data is divided into four classifications:

- SNAP diagnostics data (Figure A1-2)
- TRACE diagnostics data (Figure A1-3)
- SPM DUMP diagnostics data (Figure A1-4)
- MM DUMP diagnostic data (Figure A1-4)

The five data cards which must always be included as part of this data deck are marked with an asterisk.

## C. Target Computer Definition Data

The target computer architectural parameters which may be specified by the user are given specific values in this set of data cards. The present version of the SUMC simulator allows user specification of eleven simulation variables and the eight data cards which input these variables are described in Figure A1-5. All eight data cards must be present for proper program execution.

LAST SNAP DATA	1.5	SNAP = T > SNAP DIAGNOSTICS,	DSTICS, F > NO SNAP DIAGNOSTICS
CARD IF SNAP = F	LS	A   11	FULL SNAP WANTED; F → NO FULL SNAP
	15	RY LOC	PPED FOR FULL SNAP
ONLY WHEN FSNAP = T	5	91	*** TARGET MEMORY LOCATIONS (UP TO NINE) FOR FULL SNAP
CARD IF FSNAP = T	٦٤	TISNAP = T & TIME INTE	TIME INTERVAL SNAP WANTED; F ⇒ NO TIME INTERVAL SNAP
	15	# MEMORY LOCATIONS SN.	# MEMORY LOCATIONS SNAPPED FOR TIME INTERVAL SNAP
ONLYWHEN TISNAP =T	T AANS	SNAP TIME INTERVAL (F 12.3)	START TIME (F12.3) SNAP STOP TIME (F12.3)
	91	91	••• TARGET MEM. LOC.'S (UP TO NINE) FOR TIME INTERVAL SNAP
	ST.	KSNAP = T \$ KEYED SN.	KEYED SNAP DIAGNOSTICS WANTED; F → NO KEYED SNAP DIAGNOSTICS
CARD IF KSNAP = F	د5	PCSNAP = T → PROGCh	> PROGCNTRKEYED SNAP WANTED; F ⇒ NO PROGCNTRKEYED SNAP
	15	# PROGCNTR. SNAP KEYS (UP TO NINE)	S (UP TO NINE)
	91	14 PROG-CNT	PROG_CNTR SNAP KEY (1); # LOCATIONS TO BE SNAPPED (UP TO NINE)
	91	91	••• TARGET MEM LOC'S FOR PROG_CNTR SNAP KEY (1)
ONLY WHEN PCSNAP = T			•••
I	91	14 PROG-CNT	PROG-CNTR SNAP KEY (N); # LOCATIONS TO BE SNAPPED (UP TO NINE)
-4	91	91	••• TARGET MEM LOC'S FOR PROG-CNTR SNAP KEY (N)
	LS	OCSNAP = T > OP-CODE	♦ OP-CODE-KEYED SNAP WANTED; F ♦ NO OP-CODE-KEYED SNAP
	25	S S	TO NINE)
	4-	14 OP-CODE SNAP	OP-CODE SNAP KEY(1); # LOCATIONS TO BE SNAPPED (UP TO NINE)
	2	91	••• TARGET MEM LOC'S FOR OP-CODE SNAP KEY (1)
ONLY WHEN OCSNAP = T			•••
	4	14 OP-CODE SNAP	CODE SNAP KEY (N); # LOCATIONS TO BE SNAPPED (UP TO NINE)
	92	91	••• TARGET MEM LOC'S FOR OP-CODE SNAP KEY (N)
	۲۶	TSNAP = T + TIME - KEY	→ TIME_KEYED SNAP WANTED, F → NO TIME _KEYED SNAP
	51	SNAP	NINE)
	TIME SN.		14 TIME KEY (1); # LOC'S TO BE SNAPPED (UP TO NINE)
	92	91	••• TARGET MEM LOC'S FOR TIME SNAP KEY (1)
ONLY WHEN TSNAP = T			••
	TIME SNAP KEY,	AP KEY, MSEC (F12.3)	14 TIME KEY (N); # LOC'S TO BE SNAPPED (UP TO NINE)
,			

FIGURE A1-2. (CON'T)

	LS MASNAP ≈ T → MEM_ADDR-KEYED SNAP WANTED, F → NO MEM_ADDR-KEYED SNAP
	IS # MEM ADDR SNAP KEYS (UP TO NINE)
	16 I4 MEM ADDR'SNAP KEY (1); # LOCATIONS TO BE SNAPPED (UP TO NINE)
	16 16 TARGET MEM LOC'S FOR MEM ADDR SNAP KEY (1)
ONLY WHEN MASNAP = T	
	16 MEM ADDR SNAP KEY (N) ; # LOC'S TO BE SNAPPED (UP TO NINE)
	16 16 TARGET MEM LOC'S FOR MEM ADDR SNAP KEY (N)
, '	LS RASNAP = T > REG-ADDR-KEYED SNAP WANTED; F > NO REG-ADDR-KEYED SNAP
	IS # REG ADDR SNAP KEYS (UP TO NINE)
	14 REG ADDR SNAP KEY (1); # LOC'S TO BE SNAPPED (UP TO NINE)
	16 16 TARGET MEM LOC'S FOR REG ADDR SNAP KEY (1)
ONLY WHEN RASNAP =T	
	14 REG ADDR SNAP KEY (N); # LOC'S TO BE SNAPPED (UP TO NO (UP TO NINE)
	16 16 TARGET MEM LOC'S FOR REG ADDR SNAP KEY (N)
, 	LS MOSNAP = T SMEM-OPRND-KEYED SNAP WANTED; F & NO MEM-OPRND-KEYED SNAP
-5	17
	  -
	16 16 TARGET MEM LOC'S FOR MEM OPRND SNAP KEY (1)
ONLY WHEN MOSNAP = T	
	16 OPRND ADDR (N); OPRND KEY (N); # LOC'S TO SNAP
	16 TARGET MEM LOC'S FOR MEM OPRND SNAP KEY (N)
	LS ROSNAP = T > REG-OPRND-KEYED SNAP WANTD WANTED, F > NO REG-OPRND-KEYED SNAP
	IS # REG OPRND SNAP KEYS (UP TO NINE)
	16 011 14 OPRND ADDR (1); OPRND KEY (1); # LOC'S TO SNAP
	16 10 TARGET MEM LOC'S FOR REG OPRND SNAP KEY (1)
ONLY WHEN ROSNAP=T	
	16 011 14 OPRND ADDR (N); OPRND KEY (N); # LOC'S TO SNAP
	16 16 TARGET MEM LOC'S FOR REG OPRND SNAP KEY (N)
,	
	WILLIAM TRACE DIAGNOSTIC DATA

LAST TRACE DATA	LS TRACE = T & TRACE DIAGNOSTICS; F & NO TRACE DIAGNOSTICS *
CARD OF TRACE = F	1
LAST TRACE DATA	TITRAL = TOTIME-INTERVAL TRACE WANTED
THEN TITRACE = 1	TRACE TIME INTV, mSEC (F12.3) TRACE START TIME, mSEC (F12.3) TRACE STOP TIME, mSEC (F12.3)
	LS KTRACE = T > KEYED TRACE DIAGNOSTICS WANTED; F > NO KEYED TRACE DIAGNOSTICS
CADD IF KTRACE F	LS PCTRAC = T \$PROG_CNTR_KEYED TRACE WANTED, F \$NO PROG_CNTR_KEYED TRACE
	15 # PROG-CNTR TRACE KEYS (UP TO NINE)
	16 14 PROG CNTR TRACE KEY (1); # CONSEC INSTR'S TRACED
ONLY WHEN PCTRAC = T	
	16 14 PROG CNTR TRACE KEY (N); # CONSEL INSTR'S TRACED
	LS OCTRAC = T > OP-CODE-KEYED TRACE WANTED; F > NO OP-CODE-KEYED TRACE
	IS # OP-CODE TRACE KEYS (UP TO NINE)
	14 14 OP CODE TRACE KEY (1); # CONSEL INSTR'S TRACED
ONLY WHEN OCTRAC = T	7
I-	
6	
	14 I4 OP CODE TRACE KEY (N); # CONSEL INSTR'S TRACED
	LS TTRACE = T \$ TIME-KEYED TRACE WANTED, F \$ NO TIME KEYED TRACE
	IS # TIME TRACE KEYS (UP TO NINE)
	F12.3
ONLY WHEN TTRACE =T	
	F12.3 TIME TRACE KEY (N); # CONSEL INSTR'S TRACED
	LS MATRAC = T - MEM-ADDR-KEYED TRACE WANTED, F - NO MEM-ADDR-KEYED TRACE
	IS # MEM ADDR TRACE KEYS (UP TO NINE)
	16 14 MEM ADDR TRACE KEY (1); # CONSEC INSTR'S TRACED
ONLY WHEN MATRAC =T-	
	14 MEM ADDR TRACE KEY (N); # CONSE
	15 #REG ADDR TRACE KEYS (UP TO NINE)
ONLY WHEN RATRAC = T	IA REG ADDR TRACE KEY (1); # CONSEC INSTR'S TRACED

	14	14 REG ADDR TRACE KEY (N); = CONSEC INSTR'S TRACED	4SEC INSTR'S TRACED
	רכ	MOTRAC = T > MCM-OPRND-KEYED TRAC	♦ MCM-OPRND-KEYED TRACE WANTED; F ♦ NO MEM-OPRND-KEYED TRACE
	15	# MEM OPRND TRACE KEYS (UP TO NINE)	
	91	110	14 OPRND ADDR (1); OPRND KEY (1); # CONSEC INSTR'S
ONLY WHEN MOTRAC=T			
	91	011	14 OPRND ADDR (1); OPRND KEY (1); # CONSEC INSTR'S
•	ST	ROTRAC = T >REG-OPRND-KEYED TRACE	⇒REG-OPRND-KEYED TRACE, F → NO REG-OPRND-KEYED TRACE
	15	# REG OPRND TRACE KEYS (UP TO NINE)	
	91	110	14 OPRND ADDR (1); OPRND KEY (1); # CONSEC INSTR'S
ONLY WHEN ROTRAC = T			
	91	110	14 OPRND ADDR (1); OPRND KEY (N); # CONSEC INSTR'S
<b>,</b>		BEGIN SPM DUMP DIAGNOSTIC DATA	GNOSTIC DATA

FIGURE A1-3, (CON'T)

-	1 CULTY 3 02 CU	
2		SPM DUMP
15	# PROG CNTR SPM DUMP KEYS (UP TO NINE)	
16	16 PROG CNTR DUMP KEY (1); PROG CNTR DUMP KEY (2)	•
57	OLSPMD=T→OP-CODE-KEYED SPM DUMP WANTED; F→NO OP-CODE -KEYED SPM DI	мР
15	# OP CODE SPM DUMP KEYS (UP TO NINE)	
91	16 OP CODE DUMP KEY (1); OP CODE DUMP KEY (2);	
57	MASPMD = T → MEM-ADDR-KEYED SPM DUMP WANTED; F → NO MEM-ADDR-KEYED	IPM DUMP
51	# MEM ADDR SPM DUMP KEYS (UP TO NINE)	
91	16 MEM ADDR DUMP KEY (1); MEM ADDR DUMP KEY (2);	
LS	RASPMD = T = REG-ADDR-KEYED SPM DUMP WANTED; F = NO REG-ADDR-KEYED SF	A DUMP
51	#REG ADDR SPM DUMP KEYS (UP TO NINE)	
91	16REG ADDR DUMP KEY (1); REG ADDR DUMP KEY (2);	
LS	TSPMD = T → TIME-KEYED SPM DUMP WANTED; F → NO TIME-KEYED SPM DUMP	
Si	# TIME SPM DUMP KEYS (UP TO NINE)	
TIME DUM	MP KEY (1), mSEC(F12.3) TIME DUMP KEY (2), mSEC (F12.3)	
L5	= T DMEM-OPRND-KEYED SPMD WANTED; F	DUMP
15	# MEM OPRND SPM DUMP KEYS (UP TO NINE)	
DPRND ADDR (1)	OPRND KEY (1) (011) OPRND ADDR (2) (16)	(2) (011)
1.5	RDSPMD = T →REG-P REG-OPRND-KEYED SPM DUMP WANTED, F → NO REG-OPF	NO REG-OPRND-KEYED SPM DUMP
51	# REG OPRND SPM DUMP KEYS (UP TO NINE)	
JPRND ADDR (1)	OPRND KEY (1) (011) OPRND ADDR (1) (16) OPRND KEY	
LS	BLMMD = T > BLOCK MM DUMP(S) WANTED; F > NO BLOCK MM DUMPS	*
15	# BLOCK MM DUMP KEYS (UP TO NINE)	
91	16 PROG CNTR DUMP KEY (1), BLOCK DUMP ST	RT ADDR (1); # LOC'S DUMPED
51	16 14 PROG ENTR DUMP KEY (N); BLOCK DUMP ST	RT ADDR (N); LOC'S DUMPED
<b>L</b> S	FMMD = T > FULL MM DUMP WANTED AT END OF PROG, F > NO FULL MM DUMP	
	END OF DIAGNOSTICS DATA	
	15 16 16 16 16 16 16 16 18 18 18 18 18 18 18 18 18 18 18 18 18	# PROG CNTR SPM DUMP KEYS (UP TO NINE)   16

FIGURE A1-4. LAYOUT OF SPM DUMP AND MM DUMP DATA DECKS.

	7		7	7	7	7	7	XIIIX
HOST COMPUTER WORD LENGTH; TARGET COMPUTER WORD LENGTH	SPM SIZE; MAIN MEMORY SIZE	LOW MM ADDRESS, HIGH MM ADDRESS	TARGET PROGRAM FIRST INSTRUCTION ADDRESS		EGISTER	שא	THE (MIN)	BEGIN TARGET COMPUTER MEMORY MAP DATA
HOST COMPUTER WORD LENGTH	IIO SPM SIZE	110	TARGET PROGR	OF FIRST SPM GENERAL REGISTER	OF FIRST SPM FLOATING-POINT REGISTER	OF FIRST SPM TEMPORARY REGISTER	MAXIMUM TARGET PROGRAM EXECUTION TIME (MIN)	BEGIN TAI
13		011	011	OFFSET OF F	OFFSET OF F	OFFSET OF F	MAXIMU	
13	14			14	14	14	14	

## D. Target Computer Memory Map

The target program is defined for the simulator by specifying the memory map for the SUMC target computer. This is presently done by means of the memory map card deck which supplies memory data to the simulator on a single location per card basis. Each card contained in the memory map deck includes:

- SUMC MM address in hexadecimal
- contents of the specified MM address in hexadecimal
- number of halfwords being specified (1 or 2)

Figure A1-6 illustrates the card layouts to be used for the memory map deck. Note that the first data card must specify an offset which can be used to relocate the target memory map with respect to location zero of simulated SUMC main memory. If the offset is zero, the MM address specified in the data represent absolute addresses.

2	*. (* .* . 1)	PROGRAM OFFICE (WITH RESPECT TO ADDRESS ZEND)	ברו וס	AUDRESS ZENO)	
A6	<b>1909</b>	Α9	11		
98	8888	49	l 8		,
98	8888	Α9	B	Š	
A6	8888	Α9	B 1.1		
TARGET MEMORY ADDRESS (HEXADECIMAL)		CONTENTS OF MEMORY LOCATION (HEXADECIMAL)	Ţ	1 => HALFWORD 2 => FULLWORD	

# APPENDIX II. MODULE DESCRIPTIONS

This appendix provides a brief description of all program modules making up the complete SUMC interpretive simulator program. The material is organized so that each program module is described on a single page, and the information provided with each module description includes:

- procedure or module identifier
- purpose of the module
- programming approach
- external procedures referenced by the module.
- external data referenced by the module

Procedure Identifier: COR 001

Purpose: Mainline program for interpretive simulator.

Approach: Program is a series of subroutine calls and error checks. Snap, Dump, Trace requests are checked and executed after initialization is completed. Interrupt detection logic follows. After interrupts are serviced the computer instruction is interpretively executed. This procedure is repeated until an end of program test is successful.

External Procedure Referenced: Subroutines: COR 008 (INITLZ),
TRACSR (TRACEX), SNAPSR (SNAPEX), SPMDSR (SPMDEX), BMMDSR (BLMDEX),
COR 003 (FECHM), COR 005 (OPDEF), COR 014 (TIMER), COR 015 (INTRPS),
COR 013 (TERMIN)

External Data Referenced: Block data subprogram, input parameters.

Procedure	Identifier:	COR 002		· .	·	
Purpose:	Block data	subprogram	provides	initializ	ation of	parameters.
				• •	·	e e e e e e e e e e e e e e e e e e e
,						
			•			

Approach:

# External Procedure Referenced:

Procedure Identifier: COR 003 (FECHM)

<u>Purpose</u>: Extract current Op Code from instruction. Select Op Code dependent parameters for parse, execution time, and statistics dump. Parse instruction, perform error checking on results of parse.

Approach: Using the Op Code extracted from the instruction as a pointer, tabular values of the number of halfwords, segments/halfword, and bits/ segment are accessed. These data are utilized to extract each instruction segment and store it in the segment table for use by other subprograms.

External Procedure Referenced: BRCHK, FLD, ERINS, HALTE

Procedure Identifier: COR 004 (STATDP)

Purpose:	Publish run data summary.	
	• .	
	•	
	·	
	This subroutine accumulates and upda program execution and prints final re	
	tistics are kept concerning number of	
type of in	structions processed, and times for ea	
•		
	,	
,	·	
	•	
		·
		y in
External E	Procedure Referenced:	

Procedure Identifier: COR 005 (OPDEF)

<u>Purpose:</u> To take Op Code and parse data from COR 003 and interpretively execute the Op Code by means of a sequence of simulation instructions.

Approach: In the execution sequence, error checks are routinely done simulating the error checking facilities of the SUMC. A computed GO TO sends program control to the proper instruction simulation routine according to the value of the current instruction Op Code.

External Procedure Referenced: BRCHK, INTRPS, IOR, HALTE, FECHFW, IPPSW, FLD, JEKCC, INTROT, IER, STORCH, ERINS, IAND, OVERFL

<u>Purpose:</u> To perform a validity check upon the main storage address (MSA) furnished in COMMON variable IDATAS.

Approach: CALL BRCHK(J) where J is the integer variable set to 1 if the MSA is valid and 2 if the MSA is invalid. The main storage address must be stored in IDATAS prior to the subroutine call.

External Procedure Referenced: INTRPS

Procedure Identifier: COR 007 (STORFW)

<u>Purpose:</u> To store in main storage the full word, halfword, or character in the address provided in the call sequence.

Approach: CALL STORFW (Address, & default \$NO)

CALL STORHW (Address, & default SNO)

CALL STORCH (Address, & default SNO)

The full word, halfword or character must be previously entered in IDATAS (right justified).

External Procedure Referenced: FLD, IAND

Procedure	Identifier:	COR 008	(INITLZ)

<u>Purpose:</u> Perform the required parameter initialization for the simulator. Input the required data.

Approach: For simulation data which must be supplied by the user, FORTRAN READ statements are employed. BLOCK DATA statements provide values for internal simulation variables. Certain parameters are defined through EQUIVALENCE statements.

External Procedure Referenced:

		•
	•	

<u>Purpose:</u> Output error messages for hardware failures. Cause interruption to occur in a manner similar to SUMC hardware exceptions.

Approach: IERFLG must be set to the code that indicates the error mode.

External Procedure Referenced: INTRPS

Procedure Identifier: COR 009 (ERINS)

Procedure I	dentifier	: COR	010 (HALT	E)	
Purpose: due to fail					

.

Approach:

External Procedure Referenced:

Procedure Identifier: COR 011 (FECHFW)

Purpose: To fetch a datum from main storage.

Approach: CALL FECHFW (Address, & default SNO) full word CALL FECHHW (Address, & default SNO) halfword CALL FECHAR (Address, & default SNO) character

Datum is returned in IDATAS (right justified). Full word, halfword, character. Validity check is done on the MSA.

External Procedure Referenced: BRCHK, FLD, IAND

Procedure Identifier: COR 012 (JEKCC)

Purpose: To test the status of the condition codes.

Approach: FUNCTION JEKCC (MASK = ICODE). If any bit in the mask matches the condition code, JEKCC = 2. If no bits match, JEKCC = 1.

External Procedure Referenced: IAND

Procedure Identifier: COR 013 (TERMIN)

<u>Purpose:</u> To output message indicating successful conclusion of simulation and to institute restart subprogram if required.

Approach: A printout is initiated which identifies the termination cause and the STATDP routine is CALLED in order to print appropriate end-of-run statistics.

External Procedure Referenced: STATDP, RSTART

Procedure Identifier: COR 014 (TIMER)

<u>Purpose</u>: To maintain simulated elapsed execution time. If expected elapsed time is exceeded, simulation is terminated.

Approach: Elapsed time is incremented using parameters fetched using op code as a printer. Operations counter is incremented. Elapsed time is compared with Time Limit. If time limit is exceeded, simulation is terminated.

External Procedure Referenced: TERMIN

Procedure Identifier: COR 015 (INTRPS)

Purpose: To simulate SUMC interrupt capability.

Approach: Tables of current pending interrupts are maintained and searched upon request. An active enabled interrupt causes the appropriate service subprogram to be called. The service subprograms are not part of this contract.

CALL PUSH (priority level, interruption code, channel status, default SNO) CALL PULL (priority level, J, interruption code, channel status word) J=1 No active interrupt at this level.

J = 2 Active interrupt.

External Procedure Referenced: IMMPSW, TERMIN, HALTE, ISPPSW, IAND, ERINS

Procedure Identifier:	COR (	)16	(RSTART)
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<u>Purpose:</u> To provide facility for the restart procedures that may be added at a later date.

Approach:

External Procedure Referenced:

Procedure Identifier: COR 017 IAND (I,J)
COR 018 IOR (I,J)
COR 019 IER (I,J)

<u>Purpose:</u> To provide the logical operations of And, Or, and Exclusive OR on computer words.

<u>Approach</u>: The functions are implemented in a completely host-machine-independent manner.

External Procedure Referenced: AND, OR

TIOCEGUIE IGENETITEE! OOK OND (LONOTION THE DAKE	Procedure	Identifier:	COR	020	(FUNCTION	IMMPSW (K	()	)
--	-----------	-------------	-----	-----	-----------	-----------	----	---

<u>Purpose:</u> Converts current PSW's to old PSW formats and stores in appropriate main storage locations.

Approach: K is the address in main storage of the 1st PSW of the group. The main storage address is checked for validity.

External Procedure Referenced: BRCHK, FLD, INTRPS

Procedure Identifier: COR 021 (FUNCTION ISPPSW(K))
Purpose: To convert new PSW's in main storage into current PSW format and store into simulated scratch pad memory.
Approach: K is address in main storage of 1st PSW required. Main Storage address is checked for validity.
External Procedure Referenced: INTRPS, BRCHK, FLD

Procedure Identifier: COR 022 (FUNCTION INTNOT(K))

Purpose: To provide 1's complement of variable K

Approach: The implementation stresses host-machine-independence.

External Procedure Referenced: COMPL

Procedure Identifier: COR 023 (INTSER)	
Purpose: To provide facility for the addition of interr routines at a later date.	upt service
Approach:	
External Procedure Referenced:	
External Data Referenced:	

Procedure Identifier: COR 024 (TTWTSM(I))
COR 025 (ISMTWO(I))

Purpose: To provide function subprogram which perform conversion operations form 2's-complement representation to sign-magnitude (ITWTSM) and sign-magnitude to 2's-complement (ISMTWO).

Approach: The routines are intended for use in simulating a 2's-complement arithmetic target computer on a host system which employs sign-magnitude arithmetic.

External Procedure Referenced: IAND, IOR, INTNOT, ILOAD

Procedure Identifier:	COR 026	(ISTORE	(ISOR, IDEST, IS, IN))	

<u>Purpose</u>: To provide a host-independent routine for placing a right-justified field of data from the source word in the specified field of the destination word.

Approach: ISOR and IDEST specify the data source word and destination word, respectively. The field of data is stored in the destination word starting at bit position IS and is IN bits in length. Bit numbering is right to left with the rightmost bit designated as bit number one.

External Procedure Referenced: FLD

Procedure Identifier: COR 027 (JEXBIN (IBUF, IST, ILNG))

<u>Purpose:</u> To convert character strings in hexadecimal format to an internal IBM 7094 binary format.

Approach: IBUF is the character string location, IST is a pointer to the first character in the string IBUF, and ILNG specifies the number of hexadecimal characters to be converted. A maximum of 80 characters may be converted by the function.

External Procedures Referenced: ILOAD

Procedure Identifier: C	OR 028	(ILOAD	(SOURCE,	SB,	NB))
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<u>Purpose:</u> To provide a host-machine-independent routine for loading a field of data as a right-justified field in the output argument.

Approach: The data source word is specified by SOURCE. The field of data to be loaded as the right-justified output argument begins at bit position SB of the source word and is NB bits in length. Bit numbering is right to left with the rightmost bit designated as bit number one.

External Procedure Referenced: FLD

Procedure	Identifier:	١٠ ,	COR	029	(ISHADR(K))

Purpose: To extract the shift count from the current target instruction.

Approach: ISHADR is an integer function subprogram which is useful in executing several different target computer instructions.

External Procedure Referenced: ILOAD

Procedure Identifier: COR 030 (IVERFL(L,LOF))

<u>Purpose</u>: To compute overflow for conventional arithmetic operations based on signs of inputs and results.

Approach: Rules for generation of overflow are applied.

External Procedure Referenced: IAND

External Data Referenced: L is result of arithmetic operation; LOF is overflow parameter returned. LOF = 1  $\implies$  O/F, LOF = 2  $\implies$  No O/F.

Procedure Identifier: COR 031 (ISLOGE(N))

Purpose: To collect COMMON logic associated with SS logical instructions.

Approach: N/A

External Procedure Referenced: FECHAR, IAND, IER, IOR, STORCH

External Data Referenced: COMMON, N is call parameter defining logical operation,

N = 1, logical AND

N = 2, logical OR

N = 3, exclusive OR

Procedure Identifier: COR 032 (IOVRFL(N,J))

Purpose: To compute overflow based on logical arithmetic operations.

Approach: Special rules for logical overflow are applied to inputs and results of operations.

External Procedures Referenced: IAND

External Data Referenced: COMMON, N, J

N is result of operation, J is parameter which defines O/F.  $J = 1 \implies$ overflow;  $J = 2 \implies$  no O/F.

Procedure Identifier: Co	OR 033 (	(ICOMP1 (	(WRDIN,SB,	NB))
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<u>Purpose:</u> To provide a host-machine-independent routine for complementing a specified field of bits in the source word.

Approach: WRDIN is the source word and the function subprogram complements NB bits of this word beginning at bit position SB. Bit numbering is right to left with the rightmost bit designated as bit number one.

External Procedure Referenced: ILOAD, ISTORE

TYPESP

Procedure Identifier:

External Data Referenced:

	classification of all valid target to diagnostics keys which may be checke
compater instructions according	to diagnostics keys which may be enecked
	nstruction is assigned to a particular
classification which groups ins priateness of their contents in	tructions in accordance with the approchecking diagnostics keys.
principle of their contents in	endering drughosses heye.
•	
External Procedure Referenced:	

/DVAR/

Procedure Identifier: HEADSR (HEADER)

<u>Purpose:</u> Printout of target machine status information which serves as a header for diagnostics information which has been requested. This header will be common to all types of diagnostics.

Approach: When the mainline routine has recognized a diagnostics request, the header subroutine is called just prior to the calling of the appropriate subroutine to execute the diagnostic printout. This routine provides the user with information concerning the diagnostic requested, program time, program offset and current instruction contents.

# External Procedure Referenced:

External Data Referenced: /DVAR/, /UNCON/, /UARRAY/

blocedure Identifiet: SMarky (SMark	Procedure	Identifier:	SNAPRS	(SNAPRD
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<u>Purpose</u>: Routine to read external data which are used as keys to trigger main memory SNAP diagnostic at desired time during simulation. Each SNAP key triggers a printout of a unique set of main memory locations.

Approach: Each SNAP key specifies (1) type of key, (2) value of key, and (3) memory locations to be snapped.

# External Procedure Referenced:

External Data Referenced: /FS/, /KS/

Procedure Identifier: TRACRS (TRACRD)

<u>Purpose</u>: Routine to read external data which are used as keys to trigger the register TRACE diagnostic at desired time during simulation. Each trace key triggers a printout of the same key registers from SPM.

Approach: Each TRACE key specifies (1) type of key, and (2) value of key.

# External Procedure Referenced:

External Data Referenced: /TR/, /KT/

Procedure Identifier: SPMDRS (SPMDRD)

<u>Purpose</u>: Routine to read external data which are used as keys to trigger a dump of the SPM contents at the desired time during the simulation. Each TRACE key triggers a printout of the contents of all registers in simulated SPM.

Approach: The SPM dump key specifies (1) type of key, and (2) value of key.

External Procedure Referenced:

External Data Referenced: /SP/, /MM/

Procedure Identifier: MMDRSR (MMDRD)

<u>Purpose</u>: Routine to read external data which are used as keys to trigger a block main memory dump diagnostic at the desired time during the simulation. Each main memory block dump key triggers a printout of a unique block of contiguous main memory locations.

Approach: Each main memory block dump key specifies the value of the simulated program counter which is to be used to trigger the block dump.

External Procedure Referenced:

Procedure Identifier: SNAPSR (SNAPEX)

<u>Purpose:</u> Routine which checks SNAP keys prior to execution of each instruction and collects the desired SNAP diagnostics data if triggered.

Approach: The present version of the subroutine issues a printout of SNAP data when triggered. Subsequent versions will have provisions for collecting and storing SNAP data for printout at some later time.

External Procedure Referenced: HEADSR (HEADER)

External Data Referenced: /FS/, /KS/, /DVAR/, /UNCON/, /UARRAY/

Procedure Identifier: TRACSR (TRACEX)

<u>Purpose:</u> Routine which checks TRACE keys prior to execution of each instruction and collects the desired TRACE diagnostics data if triggered.

Approach: The present version of this subroutine issues a printout of the contents of key registers when triggered. Subsequent versions will have provisions for collecting and storing TRACE data for printout at some later time.

External Procedure Referenced: HEADSR (HEADER)

External Data Referenced: /TR/, /KT/, /DVAR/, /UNCON/, /UARRAY/

Procedure Identifier: SPMDSR (SPMDEX)

<u>Purpose</u>: Routine which checks SPM dump keys prior to execution of each instruction and collects the desired SPM contents if triggered.

<u>Approach:</u> The present version of this subroutine issues a printout of SPM contents when triggered. Subsequent versions will have provisions for storing current SPM contents for printout at some later time.

External Procedure Referenced: HEADSR (HEADER)

External Data Referenced: /SP/, /MM/, /DVAR/, /UNCON/, /UARRAY/

Procedure Identifier: BMMDSR (BLMDEX)

<u>Purpose</u>: Routine which checks the block main memory dump keys prior to execution of each instruction and collects the desired target main memory location contents if triggered.

Approach: A block dump of a specified set of target main memory locations can be triggered only by specified values of the simulated program counter. The present version of the simulator issues a printout of the specified target main memory contents when triggered. Subsequent versions will store the current contents of the target main memory locations for printout at some later time.

External Procedure Referenced: HEADSR (HEADER)

External Data Referenced: /SP/, /MM/, /DVAR/, /UNCON/, UARRAY/

Procedure Identifier: FMMDSR (FMMDEX)

<u>Purpose</u>: Routine which checks the main memory dump key prior to termination of the simulation run, and executes a full target main memory dump if requested.

Approach: A full target main memory dump is available only at the termination of a simulation program. The dump may be executed following an error termination or following a normal program halt.

#### External Procedure Referenced:

External Data Referenced: /SP/, /MM/, /DVAR/, /UNCON/, /UARRAY/

# APPENDIX III. SUMC INSTRUCTIONS

This appendix gives a brief description of each of the SUMC Bread-board System instructions which are presently implemented on the SUMC interpretive simulator.

#### GROUP I INSTRUCTIONS

Op Code	Mnemonic	Type	Instruction
04	SPM	RR	Set Program Mask

<u>Description</u>: Bits 2-7 of the general register specified by the  $R_1$  field replace the condition code and the program mask bits of the current PSW. Bits 0, 1, and 8-31 of the register specified by the  $R_1$  field are ignored. The contents of the register specified by the  $R_1$  field remain unchanged.

Op Code	Mnemonic	Type	Instruction
05	BALR	RR	Branch and Link

<u>Description</u>: The right-most 32 bits of the PSW, including the updated instruction address, are stored as link information in the general register specified by R<sub>1</sub>. Subsequently, the instruction address is replaced by the branch address. The branch address is determined before the link information is stored.

Op Code	Mnemonic	•	<u>Type</u>	Instruction
06	BCTR	•	RR	Branch on count

<u>Description</u>: The content of the general register specified by R<sub>1</sub> is algebraically reduced by one. When the result is zero, normal instruction sequencing proceeds with the updated instruction address. When the result is not zero, the instruction address is replaced by the branch address. The branch address is determined prior to the counting operation.

Op Code	Mnemonic	<u>Type</u>	Instruction
07	BCR	RR	Branch on condition

<u>Description</u>: The updated instruction address is replaced by the branch address if the state of the condition code is as specified by the contents of the R<sub>1</sub> field; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Op Code	Mnemonic	<u>Type</u>	Instruction
0A	SVC	RR	Supervisor call

<u>Description</u>: The instruction causes a supervisor-call interruption with the  $R_1$ ,  $R_2$  field of the instruction providing the interruption code.

Op Code	Mnemonic	Type	<u>Instruction</u>
10	LPR	RR	Load positive

<u>Description</u>: The absolute value of the second operand is placed in the first operand location. The operation includes complementation of negative numbers; positive numbers remain unchanged.

Op Code	Mnemonic	Type	Instruction
11	LNR	RR	Load negative

<u>Description</u>: The 2's-complement of the absolute value of the second operand is placed in the first operand location. The operation complements positive numbers; negative numbers and zero remain unchanged.

Op Code		Mnemonic	Type	<u>e</u>	Instruction
12	*	LTR	RR	L	oad and test

<u>Description</u>: The second operand is placed in the first operand location, and the sign and magnitude of the second operand determine the condition code. The second operand is unchanged.

Op Code	Mnemonic	Type	Instruction
13	LCR	RR	Load complement

<u>Description</u>: The 2's-complement of the second operand is placed in the first operand location.

Op Code	Mnemonic	Type	Instruction
14	NR	RR	AND

<u>Description</u>: The logical product (AND) of the bits of the first and second operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective AND is applied bit by bit.

Op Code	Mnemonic	Type	Instruction
15	CLR	RR	Compare logical

<u>Description</u>: The first operand is compared with the second operand, and the result is indicated in the condition code.

Op Code	Mnemonic	<u>Type</u>	Instruction
16	OR	RR	OR.

<u>Description</u>: The logical sum (OR) of the bits of the first and second operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective inclusive OR is applied bit by bit.

Op Code	Mnemonic	<u>Type</u>	<u>Instruction</u>
17	XR	RR	Exclusive OR

<u>Description</u>: The modulo-two sum (exclusive OR) of the bits of the first and second operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective exclusive OR is applied bit by bit.

Op Cods	Mnemonic	Type	Instruction
18	LR	RR	Load

<u>Description</u>: The second operand is placed in the first operand location. The second operand is not changed.

Op Code	Mnemonic	Type	Instruction
19	CR	RR	Compare

<u>Description</u>: The first operand is compared with the second operand, and the result determines the setting of the condition code. Comparison is algebraic, treating both comparands as 32-bit signed integers.

Op Code	Mnemonic	<u>Type</u>	Instruction
1A	AR	RR	Add

<u>Description</u>: The second operand is added to the first operand, and the sum is placed in the first operand location.

Op Code	Mnemonic	<u>Type</u>	Instruction
1B	SR	RR	Subtract

<u>Description</u>: The second operand is subtracted from the first operand, and the difference is placed in the first operand location.

Op Code	Mnemonic	Type	Instruction
1C	MR	RR	Multiply

<u>Description</u>: The product of the multiplier (second operand) and the multiplicand (first operand) replaces the multiplicand. Multiplier and multiplicand are 32-bit signed integers and the product is a 64-bit signed integer occupying the even/odd register pair specified by the  $R_1$  field of the instruction.

Op Code	Mnemonic	Type	Instruction
1D	DR	RR	Divide

<u>Description</u>: The dividend (first operand) is divided by the divisor (second operand) and replaced by the remainder and the quotient. The divisor is a 32-bit signed integer. The divident is a 64-bit signed integer occupying the even/odd register pair specified by the R<sub>1</sub> field

of the instruction. A 32-bit signed remainder and a 32-bit signed quotient replace the dividend in the even-numbered and off-numbered registers, respectively.

Op Code	Mnemonic	<u>Type</u>	Instruction	
1E	ALR	RR	Add logical	

<u>Description</u>: The second operand is added to the first operand, and the sum is placed in the first operand location. A carry out in the sign position is recorded in the condition code. Logical addition adds all 32 bits of both operands without further change to the resulting sign bit.

Op Code	Mnemonic	Type	Instruction	
1F	SLR	RR	Subtract logical	

<u>Description</u>: The second operand is subtracted from the first operand, and the difference is placed in the first operand location. A carry out in the sign position is recorded in the condition code. All 32 bits of both operands participate, without further change to the resulting sign bit.

Op Code	Mnemonic	<u>Type</u>	Instruction
40	STH	RX	Store halfword

<u>Description</u>: The first operand is stored at the halfword second operand location. The 16 high-order bits of the first operand are ignored.

Op Code	Mnemonic	Type	Instruction	
41	LA	RX ·	Load address	

<u>Description</u>: The address of the second operand is inserted in the low-order 24 bits of the general register specified by  $R_1$ . The remaining bits of the general register are made zero.

Op C	ode	Mnemonic	. •		<u>Type</u>	٠.	In	struction
4	2	 STC		.*	RX	;	Store	character

<u>Description</u>: Bit positions 24-31 of the register designated as the first operand are placed in the second operand address.

Op Code	Mnemonic	Type	Instruction	
43	IC	RX	Insert character	

<u>Description</u>: The 8-bit character at the second operand address is inserted into bit positions 24-31 of the register specified as the first operand location.

Op Code	Mnemonic	<u>Type</u>	Instruction
44	EX	RX	Execute

<u>Description</u>: The single instruction at the branch address is modified by the content of the general register specified by  $R_1$ , and the resulting subject instruction is executed. Bits 8-15 of the instruction designated by the branch address are  $OR^1$ ed with bits 24-31 of the register specified by  $R_1$ , except when register 0 is specified, which indicates no modification takes place.

Op Code	Mnemonic	Type	Instruction
45	BAL	RX	Branch and link

<u>Description</u>: The right-most 32 bits of the PSW, including the updated instruction address, are stored as link information in the general register specified by  $R_1$ . Subsequently, the instruction address is replaced by the branch address. The branch address is determined before the link information is stored.

Op Code	Mnemonic	<u>Type</u>	<u>Instruction</u>
46	вст	RX	Branch on count

<u>Description</u>: The content of the general register specified by  $R_1$  is algebraically reduced by one. When the result is zero, normal instruction sequencing proceeds with the updated instruction address. When the result is not zero, the instruction address is replaced by the branch address. The branch address is determined prior to the counting operation.

Op Code	Mnemonic	Type	Instruction
47	BC	RX	Branch on condition

<u>Description</u>: The updated instruction address is replaced by the branch address if the state of the condition code is as specified by the contents of the R<sub>1</sub> field; otherwise, normal instruction sequencing proceeds with the updated instruction address.

Op Code	Mnemonic	Type	Instruction
48	LH	RX	Load Halfword

<u>Description</u>: The halfword second operand is placed in the first operand location. The second operand sign bit value is propagated through the 16 high-order bit positions before insertion.

Op Code	Mnemonic	<u>Type</u>	Instruction
49	СН	RX	Compare Halfword

<u>Description</u>: The first operand is compared with the halfword second operand, and the result determines the setting of the condition code. The comparison is algebraic.

Op Code	Mnemonic	Type	Instruction
4A	AH	RX	Add halfword

<u>Description</u>: The halfword second operand is added to the first operand and the sum is placed in the first operand location. The halfword second operand is expanded to a full word before addition.

Op Code		Mnemonic	<u>Type</u>	Instruction
4B	. :	SH	RX	Subtract halfword

<u>Description</u>: The halfword second operand is subtracted from the first operand, and the difference is placed in the first operand location.

The halfword second operand is expanded to a full word before subtraction.

Op Code	Mnemonic	Type	Instruction
4C	MH	RX	Multiply halfword

<u>Description</u>: The product of the halfword multiplier (second operand) and the muliplicand (first operand) replaces the multiplicand. The halfword multiplier is expanded to a full word before multiplication and the low-order part of the product replaces the multiplicand (first operand).

Op Code	Mnemonic	Type	Instruction
4E	CVD	RX	Convert to decimal

<u>Description</u>: The radix of the first operand is changed from binary to decimal, and the result is stored in the second operand location. The number is treated as a right-aligned signed integer both before and after conversion. The result has the packed decimal format, occupies a double-word in storage, and must be located on an integral boundary.

Op Code	Mnemonic	<u>Type</u>	Instruction
<b>4F</b>	CVB	RX	Convert to binary

<u>Description</u>: The radix of the second operand is changed from decimal to binary, and the result is placed in the first operand location. The second operand has the packed decimal data format and occupies a doubleword storage field, which must be located on an integral boundary.

Op Code	Mnemonic	Type	Instruction
50	ST	RX	Store

Description: The first operand is placed in the second operand location.

Op Code	Mnemonic	<u>Type</u>	Instruction
54	N	RX	AND

<u>Description</u>: The logical product (AND) of the first and second operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective AND is applied bit by bit.

Op Code	Mnemonic	<u>Type</u>	Instruction
55	CL	RX	Compare logical

<u>Description</u>: The first operand is compared with the second operand, and the result is indicated in the condition code.

Op Code	Mnemonic	Type	Instruction
56	0	RX	OR

<u>Description</u>: The logical sum (OR) of the bits of the first and second operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective inclusive OR is applied bit by bit.

Op Code	Mnemonic	Type	Instruction
57	X	RX	Exclusive OR

<u>Description</u>: The modulo-two sum (exclusive OR) of the first and second operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective exclusive OR is applied bit by bit.

Op Code	Mnemonic	Type	Instruction
58	. L	RX	Load

<u>Description</u>: The second operand is placed in the first operand location, with the second operand left unchanged.

Op Code	Mnemonic	<u>Type</u>	Instruction
59	С	RX	Compare

<u>Description</u>: The first operand is compared with the second operand, and the result determines the setting of the condition code. The 32-bit signed integer operands are compared algebraically.

Op Code	Mnemonic Type		Instruction	
5A	A	RX	Add	

<u>Description</u>: The second operand is added to the first operand, and the sum is placed in the first operand location.

Op Code	Mnemonic	Type	Instruction
5B	S	RX	Subtract

<u>Description</u>: The second operand is subtracted from the first operand, and the difference is placed in the first operand location.

Op Code	Mnemonic	<u>Type</u>	Instruction	
5C	M	RX	Multiply	

<u>Description</u>: The product of the multiplier (second operand) and the multiplicand (first operand) replaces the multiplicand. Multiplier and multiplicand are 32-bit signed integers and the product is a 64-bit signed integer occupying the even/odd register pair specified by the  $R_1$  field of the instruction.

Op Code	Mnemonic	<u>Type</u>	Instruction
5D	D	RX	Divide

<u>Description</u>: The dividend (first operand) is divided by the divisor (second operand) and replaced by the remainder and the quotient. The divisor is a 32-bit signed integer. The divident is a 64-bit signed integer occupying the even/odd register pair specified by the R<sub>1</sub> field of the instruction. A 32-bit signed integer remainder and a 32-bit signed integer quotient replace the divident in the even-numbered and odd-numbered registers, respectively.

Op Code	Mnemonic	Type	Instruction
5E	$\mathtt{AL}$	RX	Add logical

<u>Description</u>: The second operand is added to the first operand, and the sum is placed in the first operand location. A carry out in the sign position is recorded in the condition code. Logical addition adds all 32 bits of both operands without further change to the resulting sign bit.

Op Code	Mnemonic	<u>Type</u>	<u>Instruction</u>
5 <b>F</b>	SL	RX	Subtract logical

<u>Description</u>: The second operand is subtracted from the first operand, and the difference is placed in the first operand location. A carry out in the sign position is recorded in the condition code. All 32 bits of both operands participate, without further change to the resulting sign bit.

Op Code		Mnemonic	Type	Instruction
80	٠	SSM	SI	Set system mask

<u>Description</u>: The byte at the location designated by the operand address replaces the system mask bits of the current PSW.

Op Code	Mnemonic	<u>Type</u>	Instruction
82	LPSW	SI	Load PSW

<u>Description</u>: The double word at the location designated by the operand address replaces the PSW. The operand address must be a double word address. The double word which is loaded becomes the PSW for the next sequence of instructions.

Op Code	Mnemonic	<u>Type</u>	Instruction
86	BXH	RS	Branch on index high

<u>Description</u>: An increment is added to the first operand, and the sum is compared algebraically with a comparand. Subsequently, the sum is placed in the first operand location, regardless of whether the branch is taken. When the sum is high, the instruction address is replaced by the branch address. When the sum is low or equal, instruction sequencing proceeds with the updated instruction address. The first operand and the increment are in the registers specified by  $R_1$  and  $R_3$ . The comparand register address is odd and is either one larger than  $R_3$  or equal to  $R_3$ . The branch address is determined prior to the addition and comparison.

Op Code	Mnemonic	Type	Instruction
87	BXLE	RS	Branch on index low or equal

<u>Description</u>: An increment is added to the first operand, and the sum is compared algebraically with a comparand. Subsequently, the sum is placed in the first operand location, regardless of whether the branch is taken. When the sum is low or equal, the instruction address is replaced by the branch address. When the sum is high, normal instruction sequencing

proceeds with the updated instruction address. The first operand and the increment are in the registers specified by  $R_1$  and  $R_3$ . The comparand register address is odd and is either one larger than  $R_3$  or equal to  $R_3$ . The branch address is computed prior to the addition and comparison.

Op Code	Mnemonic	<u>Type</u>	Instruction
88	SRL	RS	Shift right single

<u>Description</u>: The first operand is shifted right the number of bits specified by the low-order six bits of the second operand address field.

Zero's are shifted into vacated register positions.

<u>Op Code</u>	Mnemonic	<u>Type</u>	Instruction
89	SLL	RS	Shift left single

<u>Description</u>: The first operand is shifted left the number of bits specified by the low-order six bits of the second operand address field.

Zero's are shifted into vacated register positions.

Op Code	Mnemonic	<u>Type</u>	Instruction
8A	SRA	RS	Shift right single

<u>Description</u>: The integer part of the first operand is shifted right the number of bits specified by the low-order six bits of the second operand address field. Bits equal to the sign are supplied to vacated register positions.

Op Code	Mnemonic	<u>Type</u>	Instruction
8B	SLA	RS	Shift left single

<u>Description</u>: The integer part of the first operand is shifted left the number of bits specified by the low-order six bits of the second operand address field. Zero's are shifted into vacated register positions.

Op Code	Mnemonic	<u>Type</u>	Instruction
8C	SRDL	RS	Shift right double

<u>Description</u>: The double word first operand is shifted right the number of bits specified by the low-order six bits of the second operand address field. The R<sub>1</sub> field of the instruction must contain an even register address specifying an even/odd register pair. Zero's are supplied to vacated register positions.

Op Code	Mnemonic	<u>Type</u>	Instruction
8D	SLDL	RS	Shift left double

<u>Description:</u> The double word first operand is shifted right the number of bits specified by the low-order six bits of the second operand address field. The R<sub>1</sub> field of the instruction must contain an even register address specifying an even/odd register pair. Zero's are supplied to vacated register positions.

Op Code	Mnemonic	<u>Type</u>	Instruction
8E	SRDA	RS	Shift right double

<u>Description</u>: The double-length integer part of the first operand is shifted right the number of places specified by the low-order bits of the second operand address field. The R<sub>1</sub> field of the instruction must contain an even register address specifying an even/odd register pair. Bits equal to the sign bit are supplied to vacated register positions.

Op Code		Mnemonic	T	ре		Ins	struct	ion
8 <b>F</b>	. :	SLDA	3	RS	Sh	ift	left	double

<u>Description</u>: The double-length integer part of the first operand is shifted left the number of places specified by the low-order six bits of the second operand address field. The R<sub>1</sub> field of the instruction must contain an even register address specifying an even/odd register pair. Zero's are supplied to vacated register positions.

Op Code	Mnemonic	<u>Type</u>	Instruction
90	STM	RS	Store multiple

<u>Description</u>: The set of general registers starting with the register specified by  $R_1$  and ending with the register specified by  $R_3$  is stored at the locations designated by the second operand address. The general registers are stored in the ascending order of their addresses, starting with the register specified by  $R_1$  and continuing through the register specified by  $R_3$ , with register 0 following register 15.

Op Code	Mnemonic	<u>Type</u>	Instruction
91	TM	SI	Test under mask

<u>Description</u>: The byte of immediate data, I<sub>2</sub>, is used as an 8-bit mask to set the condition code, The bits of the mask are made to correspond one for one with the bits of the character in storage specified by the first operand address. A mask bit of one indicates that the storage bit is to be tested; when zero, the storage bit is ignored. When all storage bits thus selected are zero, the condition code is made zero. The code is also made zero when the mask is all-zero. When the selected bits are all-one, the code is made 3; otherwise, the code is made 1.

Op Code	Mnemonic	<u>Type</u>	Instruction
92	MVI	SI	Move

<u>Description</u>: The 8-bit byte immediate operand is placed in the first operand location.

Op Code	Mnemonic	Type	Instruction
93	TS	SI	Test and set

<u>Description</u>: The leftmost bit of the byte located at the first operand address is used to set the condition code, and the entire address byte is set to all ones.

Op Code	Mnemonic	Type	Instruction
94	NI	SI	AND

<u>Description</u>: The logical product (AND) of the bits of the first operand and the immediate operand is placed in the first operand location.

Operands are treated as unstructured logical quantities, and the connective AND is applied bit by bit.

Op Code	Mnemonic	Type	Instruction
95	. CLI	SI	Compare logical

<u>Description</u>: The first operand is compared with the immediate operand, and the result is indicated in the condition code.

Op Code	Mnemonic	<u>Type</u>	Instruction
96	OI	SI	OR

<u>Description</u>: The logical sum (OR) of the bits of the first and immediate operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective inclusive OR is applied bit by bit.

Op Code	•	Mnemonic	Type	Instruction
97		XI	SI	Exclusive OR

<u>Description</u>: The modulo-two sum (exclusive OR) of the bits of the first and immediate operands is placed in the first operand location. Operands are treated as unstructured logical quantities and the connective exclusive OR is applied bit by bit.

Op Code	Mnemonic		Type	Instruction
98	IM	٠	RS	Load Multiple

<u>Description</u>: The set of general registers starting with the register specified by  $R_1$  and ending with the register specified by  $R_3$  is loaded

from the locations designated by the second operand address. The general registers are loaded in the ascending order of their addresses, starting with the register specified by  $\mathbf{R}_1$  and continuing through the register specified by  $\mathbf{R}_3$ , with register 0 following register 15.

## GROUP III INSTRUCTIONS

Op Code	Mnemonic	<u>Type</u>	Instruction
D1	MVN	SS	Move numerics

<u>Description</u>: The low-order four bits of each byte in the second operand field, the numerics, are placed in the low-order bit positions of the corresponding bytes in the first operand fields. Movement is left to right through each field one byte at a time, and the fields may overlap in any desired way. The high-order four bits of each byte, the zones, remain unchanged.

Op Code	Mnemonic	<u>Type</u>	Instruction
D2	MVC	SS	Move

<u>Description</u>: The second storage operand is placed in the first storage operand location. Movement is left to right through each field a byte at a time and the fields may overlap in any desired way.

Op Code	Mnemonic	<u>Type</u>	Instruction
D3	MVZ	SS	Move zones

<u>Description</u>: The high-order four bits of each byte in the second operand field, the zones, are placed in the high-order four bit positions of the corresponding bytes in the first operand field. Movement is left to right through each field one byte at a time, and the fields may overlap in any desired way. The low-order four bits of each byte, the numerics, remain unchanged.

Op Code	<u>e</u> <u>Mnemonic</u>	<u>Type</u>	Instruction
. D4	NC	SS	AND

<u>Description</u>: The logical product (AND) of the bits of the first and second storage operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective AND is applied bit by bit.

III-19

Op Code	Mnemonic	<u>Type</u>	Instruction
D5	CLC	SS	Compare logical

<u>Description</u>: The first storage operand is compared with the second storage operand, and the result is indicated in the condition code. Comparison is binary, and all codes are valid.

Op Code	Mnemonic	<u>Type</u>	Instruction
D6	OC	SS	OR

<u>Description</u>: The logical sum (OR) of the bits of the first and second storage operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective inclusive OR is applied bit by bit.

Op Code	Mnemonic	<u>Type</u>	Instruction
D7	XC	SS	Exclusive OR

<u>Description</u>: The modulo-two sum (exclusive OR) of the bits of the first and second storage operands is placed in the first operand location. Operands are treated as unstructured logical quantities, and the connective exclusive OR is applied bit by bit.

Op Code	Mnemonic	<u>Type</u>	Instruction
DC	TR	SS	Translate

<u>Description</u>: The eight-bit bytes of the first operand are used as arguments to reference the list designated by the second operand address. Each eight-bit function byte selected from the list replaces the corresponding argument in the first operand. The bytes of the first operand are selected one by one for translation, proceeding left to right. All data is valid and the operation proceeds until the first operand field is exhausted.

Op Code	Mnemonic	<u>Type</u>	Instruction
DD	TRT	SS	Translate and test

Description: The eight-bit bytes of the first operand are used as arguments to reference the list designated by the second operand address. Each eight-bit function byte thus selected from the list is used to determine the continuation of the operation. When the function byte is a zero, the operation proceeds by fetching and translating the next argument byte. When the function byte is non-zero, the operation is completed by inserting the related argument address in general register 1, and inserting the function byte in general register 2. Fetching of the function byte from the list proceeds as in TRANSLATE. When the first operand field is exhausted before a non-zero function byte is encountered, the condition code is set to 0. The condition code is set to 1 when one or more argument bytes have not been translated. The condition code is set to 2 if the last function byte is non-zero.

Op Code	Mnemonic	Type	Instruction
F1	MVO	SS	Move with offset

<u>Description</u>: The second operand is placed to the left of and adjacent to the low-order four bits of the first operand. The fields are processed right to left. If necessary, the second operand is extended with high-order zero's. If the first operand field is too short to contain all bytes of the second operand, the remaining information is ignored.

Op Code	<u>Mnemonic</u>	<u>Type</u>	Instruction
F2	PACK	SS	Pack

<u>Description</u>: The format of the second operand is changed from zoned to packed, and the result is placed in the first operand location. The fields are processed right to left. If necessary, the second operation is extended with high-order zero's. If the first operand field is too short to contain all significant digits of the second operand field, the remaining high-order bits are ignored. Overlapping fields may occur.

Op Code	Mnemonic	<u>Type</u>	Instruction
F3	UNPK	SS	Unpack

<u>Description</u>: The format of the second operand is changed from packed to zoned, and the result is placed in the first operand location. The fields are processed right to left. The second operand is extended with high-order zero digits before unpacking, if necessary. If the first operand field is too short to contain all significant digits of the second operand field, the remaining high-order digits are ignored. Overlapping fields may occur.

## APPENDIX IV. SUMC SIMULATOR SOURCE PROGRAM

This appendix contains the complete source listing for the basic SUMC interpretive simulator. The source language is FORTRAN IV and the program has been developed for operation on an IBM 7094 host computer.

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POTRAG. COTRAC. ITRACE. LTTRAC(9), MATRAC, RATRAC, MOTRAC, ROTRAC
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LCCG,MPCS,TIMEC,NRCUCE,NSTAT,LBPS1,LBPS2,NULL,IONE,IT,
CSLAE,ILC,INTCCE,ICGUNT,EXTIME,TIMLIM,
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POSPHO, COSPMO, TOMBO, LIOK (9), MASPMO, RASPMO, MUSPMO, ROSPMO

SEA (4), \*GUK (9), RCUK ± (9), ROSK (9)

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                                                                                                                              /KS/KSNAP, PCSNAP, NPCSK, PCSK, NPCSKL, PCSLOC.
                                                                                                                                                                              MASNAP, NMASK, MASK, NMASKL, MASLOC,
                                                                                                                                                      CSNAP, NGCSK, OCSK, NOCSKL, GCSLOC,
                                                                                                                                                                                                        RASNAP,NRASK,RASK,NRASKL,RASLOC,
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                                                                                                                                                                                                                                                                                                                                                                                                                  MCTRAC, NMOTK, MOTKA, MOTK, NIMOTK,
                                                                                                                                                                                                                                                                                                                                                                                                                                            RCIRAC, NROIK, ROIKA, ROIK, NIRCIK
                                                                                                                                                                                                                                                                                                                                                                                      TTRACE, NTTK, TTK, NITTK, LTTRAC,
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ePCCK(9), BCSTAC(9), NBDL(9)
                                                                           CMMEN / FS/SNAP, FSNAP, NFSL, SLOC,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           CALL PULL (IPR, J. IPRSTA, ICSMO)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                ECUIVALENCE (ISPM(25), INACCR)
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            LCCP
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                                                 XTERNAL ITHTSM. ISMTHO
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         F'(BLMYC) CALL BLMCEX
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        (TRACE) CALL TRACEX
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COMMEN/UNCON/1FWA, 1FGST, 1TARG, IOPCW, 1BIT, IPARS, IOATAS, 1HW, MAXCOR, LCCG, MPCS, TIMEC, NRCOCE, NSTAT, LBPS1, LBPS2, NULL, 1ONE, IT.
                                                                                                                                                                               EQUIVALENCE (ISPN(25), INADDR)
EQUIVALENCE (ISYSMK, ISPN(26)), (IPRMSK, ISPN(27)), (IAWP, ISPN(29)),
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IINSPAR(5,20),IPCTR(5),IPPCTR(5),ISGCO(5,20),IADR(3),ISPM(64),
                                                                                                                                                                                                                                                                                                               COMMEN JEVAR/10PC0(255), ITCNTR, 10FFST, 10PRND(3), 1STAT
                                                                                                                                                                                                                                                                                                                                                           CR POUNDARY EXCURSION TERMINATES
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     CSLAE, ILC, INTCEE, ICGUNT, EXTIME, TIMLIM,
DATA IHCST, ITARG, 10PCW, 1811/36, 32, 8, 1/
                               ( (INSOAT(I,J), I=1,255), J=1,2
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | IHALFW(6), | STACK(5,6), | MAINM(4096)
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             Leps1, Leps2/ 30,28/
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CQUIVALENCE (18YS/K,18PM(26)),(1PMMSK,18PM(27)),(1AWP,18PM(29))
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                                        GC TG (2011;2012,2013,2014,2015,2016), IPARS
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                                                                                                                       ACR(1)=K+L+1SEGTA(11)
                                                                                                                                                                                                                                                                                                     F(1SEGTA(6).GT.0) GO
                                                                   LCCG + ISEGTA(2)
LCCG + ISEGTA(3)
                                                                                                                                                                                                                                                                                                                                             IMPA_LCCG+ISEGIA(6)
                                                                                                                                                                                                                                                ACR(1)=L+1SEGTA(11)
                                                                                                                                                                              ASR(1)=L+1SEGTA(11)
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                                                                                                                                     MM=LCCG+1SEGTA(2)
                                                                                                                                                                                                        MN=LGCG+ISEGTA(3)
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                                                                                                                                                                                          FF-LCCG+1SECTA(2)
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CMMCN/UNCCA/IFWA, IECSI, ITARG, IOPCW, IBIT, IPARS, IDATAS, IHW, MAXCOR,
                                                                                                                                                                                                                                                        COMMENJUNCONZIFMA, IFEST, ITARG, IOPEW, 181T, IPARS, IDATAS, IHW, MAXCOR,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 CUIVALENCE (ISYSMK, ISPM(26)), (IPRMSK, ISPM(27)), (IAMP, ISPM(29)),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   SVCNPS); (IMAINME 27); PRNPSW); (IMAINME 29); MANPSW); (IMAINME 31);
SUCKES), (IRELING ( 24); PRNPSE), (IRELING ( 24); MANFSE), (IRELING ( 31)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               CLASS
                                                                                                                          (IMAINH(25), SVALCC), (IMAINM( 28), PRALCC), (IMAINM( 30), MANLOC)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        INCCH2), (IMAINN("7), EXOPSW), (IMAINM( 9), SVCOPS), (IMAINM(II),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              (IMBINN(26), SVALOC), (IMBINN( 28), PRNLCC), (IMBINN( 33), MANLOC
                                                                                                                                                                                                                                                                                                                                                                                                                                      | INSPAR(5,20), | PCTR(5), | PPCTR(5), | SGCD(5,20), | ADR(3), | SPM(64),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 CUIVALENCE (IMAINM(I), INIPSW), (IMAINM(3), INCCMI), (IMAINM(5),
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                                                                                                  (IMAIN#(14), MACLOC), (IMAIN#(15), IOOLOC), (IMAIN#(24), EXNLOC)
                                                                                                                                                                                                                                                                                                                                                                                                              CCMMCN /UBRRAY/ ISECTA(20), TIME(10), CLASS(10), INSDAT(256,5),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          CSWCRD), (IMAINM(19), CAMCRD), (IMAINM(23), EXNPSW), (IMAINM(25),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               (IMAINM( 8), EXCLCC), (IMAINM(ID), SVOLOC), (IMAINM(IZ), PROLOC)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    (IMBINY (14), MACLOC), (IMAINM (15), IOGLOC), (IMAINM (24), EXNLOC)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 EXCPSW(4), SVCOPS(4), PROPSW(4), MAOPSW(4), IOOPSW(4),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      CSWCRC(4), CALCRC(4), EXNPSW(4), SVCNPS(4), PRNPSW(4), MANPSW(4)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             CNPSW), (ISPM(25), INACCR), (ISPM(25), CURPSW), (ISPM, GENREG),
                     CNPSW), (ISPM(25), INACCR), (ISPM(25), CURPSh), (ISPM, GENREL)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     (ISP*(17), FLPTRG), (ISPM(33), TSTORG), (IMAINM(1), INPRCT),
                                                                                                                                                                                                                                                                                LCCG, MPCS, TIMEO, NRCOCE, NSTAT, LBPS1, LBPS2, NULL, IONE, IT,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          LOCS, MEDS, TIMPC, VRCCCE, WSTAT, LSPS1, LSPS2, NULL, IONE, II,
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                                                                         (IMAINM( 8), EXCLOC), (IMAINM(10), SVOLOC), (IMAINM(12),
                                                 11SPM(17), FLPTRG), (1SPM(33), TSTGRG), (1MAINM(1), INPRC#
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         COMMON JEVAR/ICPCC(255), ITCNTR, 10FFST, 10PRND(3), 1STAT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         INSTRUCTION CLASS CISTRIBUTION///68H
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             OPACA /TES/ LEVELS(4), IGUTPU(5), IPOINT(5)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              EXCLGC, SVOLCC, PROLOC, EXNLOC, SVNLOC, PRNLOC
                                                                                                                                                                                                                                 CMMCN /IES/ LEVELS(4), IOUTPU(5), IPOINT(5)
                                                                                                                                                                                                                                                                                                          CSLAE, ILC, INTCCE, ICQUNT, EXTIME, TIMLIM,
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                                                                                                                                                                                                                                                                                                                                                                                                                                                              IHALFW (6), ISTACK (5,6), IMAINM (4096)
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            WRITE (6,2) SUMI, TIMBC, SUMZ
                                                                                                                                                                                                                                                                                                                                                                 LCECUN, JIROUN, MONE, IFETC
                                                                                                                                                                                                                                                                                                                                   IMM, IMM, FERFLG, IRESTA,
                                                                                                                                                        (IMAINY( 32), ICALGC)
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              SUM1=SUM1+CLASS(I)
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= K = ISTCRE(IPRMSK, ISPM(IMM), LBPS1,2) (3) - EC.0) GG TG 3CG ACCR * ISPM(IPM) - I (3) - EC.0) GG TG 3CG PM   EC.0) GG TG 3CG EC.0) EC.0) GG TG 3CG EC.0) EC.0) GG TG 3CG EC.0) EC.0) EC.0) GG TG 4CG EC.0) EC.0) EC.0) EC.0 EC.0 EC.0 EC.0 EC.0 EC.0 EC.0 EC.0	DCR R=IAND(KACR.ISPM(IMN))	
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(2).EC.O.CR.ISEGTA(3).EQ.O) GC TO (2)-11)2999,2605,3602	AS=INACOR	
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SCOTISEMITAN), KACR SCCR	A(Z)	
	RAIDUELDAMILMADAMER Salnaeer	
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F(IANC(MAXNEG, ISPM(IMN)).EG.O/ GO TO 3014
                                                                                                                                                                      IF(IANC(MAXNEG;N).EC.C) GO TO 3C08
IF(N.LE.MAXNEG) GO TO 3C19
ISPW(IMM)=INTNCT(N)+1
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C**** INITIALIZE PARAMETERS FOR ITERATIVE MULTIPLICATION
                                                                                                                                                                                                                                                                                                                                            C**** STORE PROCUCT IN SPM O RETURN TO MAINLINE ****
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                                                 F ((ICANC.EG.0).0R.(IIER.EG.0)) GO
                                                                                                                                                                                                                          CCNVERT PRODUCT IF NECESSARY #**
                                                                                                                ITERATIVE 4-BIT MULTIPLICATION
                                                                                                    F (15EGTA(1).EC.76) 1C=1TARG/8
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                                                                                                                                                                                                                                                                             F (IMAR-NE.0) GG TC 503
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                                                                                                                                            KEY= ILCAC(IIER, INB,4)
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NECESSARY O STORE IN SPM #####
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IF ((IDSK.EQ.0),OR.(IPR.EQ.0)) GO
IPR=ICGMPI(IPR.ITARG,ITARG)
IOPACI * (CCMP111CENCI, ITARG, ITARG
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IF ((ISK.NE.1).CR.(IQUO.EQ.0))
IQUO=ICCMP1(IQUC.ITARG,ITARG)
                    CHROWICH CONPICIONS, ITARG
                             (ICENCI.EC.O) ICENC=ICENC+1
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           IF(ISPA(1777,NE.0) GO TO 3110
                                                                                                   IIPR=ILCAU(ICENCI,ITARG,1)
IF (IIPR.EQ.1) ICENC=ICENC+1
                                                                                                                                         C**** PERFERM ITERATIVE EIVISION
                                                                                                                                                                                                              F (IPR-EG.1) IPR=IPR+I
F (IPR-ISGR) 505,506,506
                                                                               IF (IPR.GE.O) GC TC 1510
IDENC=2*ICeNC
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IF(1SPM(1MM),EC.0) GO TO
                                                                                                                              IF (IPR.GE.0) GC TO 1510
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L=ISPM(IMM)+ISPM(IMM)
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                                                                                                                                             FILIAND(ISPM(IMM), MAXNEG). GT.NULL) GO TO 3062
                                                                                                                                                                                                                                                                                                    GO TO3C62
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            SPM(IMM+1)=ISTCRE(ISPM(IMM+1), MM, ITARG, IA)
                                                INDV(INV+1)=ISTORE(ISDV(IMM+1), MM, ITARG,M)
                                                                                                                                                                                                                                                       ISPA(INY+1)=ISTORE(NA, ISPA(IMM+1), ITARG, 1)
                                                                                  SPM(IMM) = ISTORE(ISPM(IMM+1), MM, ITARG, LL)
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             (SOM (IMM) = ISTONE (ISPM (IMM), MM, ITANG, M) now (IMM) = ILCAC (ISPM (IMM+1), ITANG, 1)
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                                                                                                                                                                                                                                             PW=ILCAC(ISPM(IMM+1), ITARG, IA)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             STORG(I)=ILCAC(ISPM(IMM),M.I
                                                                                                                                                                                                                                                                               WM=ILCAC (ISPM (IMM) . M.K.
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                                                                                                SPM(IMM+1)=NULL
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                                                                                                                        142
                                                                                                                                    I = I SHADR (K)
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7.4	47 K=1ADR(1) CALL FECHAR(K.S	
1231	ICC=IANC(IDATAS, 128)	
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	148 L=1SEGTA(14)	
1238	CALL FECHAS(K, \$201)	
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[F(M.LT.0.CR.M.GT.255) GO TO 3002
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                                                                         :ALL STCKCH(K, $301)
F(IDATAS)3025,3026,3025
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                   CATAS= ICR(L, ICATAS
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                                                            ALL FECHAR(K, $301)
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SPM(J)=IDATAS
                         ALL STCRCH(K, $301
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COMMON/UNCON/IEWA,IHOSI,ITARG,IOPCW,IBIT,IPARS,IDATAS,IHW,MAXCOR
                                                                                                                                                                                                                                                                                                                                                                                                                                                  CCMCN /TES/ LEVELS(4), IQUIPU(5), IPOINT(5)
COMMON/UNCON/IFWA, IFOST, ITARG, IOPCW, IBIT, IPARS, IDATAS, IHW, MAXCOR
                                                                                                                                                           CGMMCN /UARRAY/ ISECTA(20), TIME(10), CLASS(10), INSDAT(256,5),
                                                                                                                                                                              13,SPAR(5,20), 1PCTR(5), 1PPCTR(5), 1SGCD(5,20),1ADR(3),1SPM(64),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          COMMON /UARRAY/ ISEGTA(20),TIME(10),CLASS(10),INSDAT(256,5),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | INSPAR(5,20), | PCTR(5), | IPPCTR(5), | ISGCO(5,20), | IADR(3), | ISPM(64)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         LOCG, MPOS, TIMBO, NRCOCE, NSTAT, LBPSI, LBPS2, NULL, IONE, IT,
                                                         LCCG, MPCS, TIMEG, NRCOCE, NSTAT, LBPS1, LBPS2, NULL, IONE, IT,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     CCMMCN /CVAR/1CPCO(255), ITCNTR, IOFFSI, IOPRNO(3), LSTAT
                                                                                                                                                                                                                       COMMON /CVAR/ICPCO(255), ITCNTR, IOFFST, IOPRNO(3), ISTAI
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              PAINM(K) = ISTORE(ILGAC(ICATAS, I, IHW), II, L, IHW)
                                                                                                                                                                                                                                            F(IDATAS.GT.MAXCGR.OR.ICATAS.LT.C) GO TO 20
                 OPMON /TES/ LEVELS(4), IOUTPU(5), IPOINT(5)
                                                                               CSLAE, ILC, INTODE, ICCUNT, EXTIME, TIMLIM,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            GSLAE, ILC, INTCDE, ICOUNT, EXTIME, TIMLIM,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        1955 E, 1001 C
PAINM(K)=ILCAD(IDATAS, ITARG, ITARG)
                                                                                                                                                                                                       IHALFW(6), ISTACK(5,6), IMAINM(4096)
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                                                                                                                                                                                                                                                                                                                                                                                                                                SUBRCUTINE STORFW(ICACR,*
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                                                                                                                      LOBCON, JISCON, MCNE, IFETC
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      LOBOUN, JI BOUN, MGNE, IFETC
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 INM, IMN, IERFLG, IRESTA,
                                                                                                   INT, INN, IERFLG, IRESTAL
                                                                                                                                                                                                                                                                                                        CALL PUSH(2,5,0, $301)
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CGICAL CSLAE, IRESTA
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                                                                                                                                             GITMU= FALSE
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                                                                                                                                                                                                                                                                                                                                                ERFLG=14
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COMMENJUNCON/ IFWA, IFOST, ITARG, IOPCH, IBIT, IPARS, IDATAS, IHH, MAXCOR
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 SVCNPS), (IMAINM ( 27), PRNPSH), (IMAINM ( 29), MANPSH), (IMAINM ( 31
                                                                                                                                                                                                                                                                                                                                                                                                                                         QUIVALENCE(IMAINMII), INIPSK), (IMAINM(3), INCCHI), (IMAINM(5),
                                                                                                                                                                                                                                                                                                                                                                                                                                                           INCCHZ), (IMAINMI 7), EXGPSW), (IMAINMI 9), SVCOPS), (IMAINMIII),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                            PROPSW), (IMAINW(13), MACPSW), (IMAINK(15), ICOPSW), (IMAINM(17),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             CSWERE), (IMAINM(19), CANORE), (IMAINM(23), EXNPSH), (IMAINM(25),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      (IMAINM( B), EXCLGC), (IMAINM(10), SVOLOC), (IMAINM(12), PROLOC).
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           (IMAINM(14), MACLOC), (IMAINM(15), 100LOC), (IMAINM(24), EXNLOC),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     COMMON / JARRAY/ ISEGTA(20), TIME(10), CLASS(10), INSDAT(256,5),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        INSPAR(5,20), IPCTR(5), IPPCTR(5), ISGCD(5,20), IADR(3), ISPM(64),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   ICNPSW), (ISPM(25), INACCR), (ISPM(25), CURPSK), (ISPM, GENREG),
                                                                                                                                                                                                                                                                                                                                           EXCPSK(4), SYCOPS(4), PROPSW(4), MACPSW(4), 100PSW(4),
                                                                                                                                                                                                                                                                                                                                                              CSWORCIA), CANORCIA), EXNPSW(4), SVCNPS(4), PRNPSW(4), MANPSW(4)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      (ISPP(17), FLPTRG), (ISPM(33), TSTORG), (IMAINM(1), INPRCT),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           LCCG, PPCS, TIMEC, NRCOCE, NSTAT, LBPS1, LBPS2, NULL, IONE, IT,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         COMMENJIR/ IRACE, FIRACE, TITRAC, IRTI, ISTRI, ISTPI, KIRACE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              COMMON /CVAR/ICPCO(255), ITCNIR, IOFFST, IOPRNO(3), ISTAT
                                                                                                                                                                                                                                                                                                                                                                                                    TSTORG(10)
                                                                                                                                                                                                                                                                                                                                                                                   EXOLCC, SVCLCC, PRCLCC, EXNLCC, SVNLOC, PRNLOC,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        COMMON /TES/ LEVELS(4), IOUTPU(5), IPDINT(5)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              CSLAE, ILC, INTCDE, ICOUNT, EXTIME, TIMLIM,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            IHALFh(6), ISTACK(5,6), IMAINM(4096)
                                                                                                                                                                                                                                                                                                                                                                                                    IGNPS#(4), CURPSW(4), GENREG(16),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   ECUIVALENCE (ISPM(25), INADOR)
                                                                                           DATAS=ILCAC(IMAINM(K),N,8)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   LCBOUN, JIBGUN, MCNE, IFETC
                                                                           N=1TARG-IANC(ICACR, 31*8
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     DATA CHALLE/4294967295/
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               GENERAL REGISTER CFFSET
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 INM, IMM, IERFLG, IRESTA.
                                                                                                                                                                                                                                                                                                         CATA M1/C7160606060559/
                                    VIRY STERCH(ICADR, *)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    (IMAINME 32), ICNLCC)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       LOGICAL OSLAE, IRESTA
                                                                                                                                                                                                                                                                                                                                                                                                                         DIMENSION FLPTAG(8)
                                                                                                                                                                                                                                                                    INTEGER 18UF(80) COMMON/8UF1/ 18UF
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            FURMAT (4110+F16+3)
                                                                                                                                                                                                                              SUPRCUTINE INITEZ
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                                                                                                                                                                                                                                                 LOGICAL TESTO1
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COMMON/UNCON/IFWA, IFOST, ITARG, IOPCW, IBIT, IPARS, IDATAS, IHW, MAXCOR, LCCG, MPCS, TIMBG, NRCOCE, NSTAT, LBPS1, LBPS2, NULL, IONE, IT.
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          COMMEN /UBRRAY/ ISEGTA(20),TIME(10),CLASS(10),INSDAT(256.5), INSPAR(5,20),IPCTR(5),IPPCTR(5),ISGCD(5,20),IADR(3),ISPM(64),
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                                                                                                                                                                                                                                                              WRITE(6,1001) LOBOUN, JIBOUN, IFWA, INACOR, TIMLIM
                       READ 1901 . LERGUN, JIBOUN, IFWA, INADOR, ILMLIM
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EQUIVALENCE (ISPM(25), INADOR)
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COPPORTING (1 IFWA, IFOST, ITARG, IOPOW, IBIT. IPARS, IDATAS, IHW, MAXCOR
LCCG, MPCS, TIMEO, NRCOCE, NSTAT, LOPSI, LBPS2, NULL, IONE, II,
                                                             INSPAR(5,23), IPCTR(5), IPPCTR(5), ISGCO(5,20), IADR(3), ISPM(64),
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COMMON /CWAR/ICPCC(255), ITCNIR, IOFFST, IOPRNO(3), ISTAT
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COMMON/DVAR/ ICPCO(255), ITCNTR, IOFFST, IOPRNO(3)
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                  NITE(6,1) INACCR, IACR(1), IOPRNO(1), IERFLG
                                     BAC INSTRUCTION, 3017, 110)
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                                                                                                                                CALL PUSF (2,1,0,5300)
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COMMICH/UNCON/IFWA, IFOST, ITARG, IOPCW, 1811, IPARS, IDATAS, IHM, MAXCOR,
                                       W WAXCOR
                                                                                                                                                            CCPMCN /UARRAY/ ISEGTA(20), TIME(10), CLASS(10), INSDAT(256,5),
                                                                                                                                                                                 INSPAR(5,20), IPCTR(5), IPPCTR(5), ISGCO(5,20), IADR(3), ISPP(64),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                INSPAR(5,201, IPCTR(5), IPPCTR(5), ISGCD(5,20), IADR(3), ISPM(64),
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         INTEGER EXOPSW(4), SVCOPS(4), PROPSW(4), MAOPSW(4), 100PSW(4),
                                                        LGGG,MPCS,TIMBC,NRCGCE,NSTAT,LBPS1,LBPS2,NULL,IONE,IT
                                     . ONMON/UNCON/IFWA, IMOST, ITARG, IOPCW, IBIT, IPARS, IDATAS
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                                                                                                                                                                                                                        DMMCN / DVAR/ICPCO(255), ITCNTR, IDFFST, IDPRND(3), ISTAT
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                    SMMCN /TES/ LEVELS(4), IOUTPU(5), IPOINT(5)
                                                                                                                                                                                                                                                                                                                                                                                                                                                COMMON /TES/ LEVELS(4), IOUTPU(5), IPDINT(5)
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                                                                              OSLAE.ILC, IRTCCE, ICCUNT, EXTIME, TIMLIM,
                                                                                                                                                                                                       LIHALFW(6), ISTACK(5,6), IMAINM(4096)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       [HALFW(6), ISTACK(5,6), IMAINM(4096)
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                                                                                                     LIMM, IMM, INRFLO, IRESTA,
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COPMON /TES/ LEVELS(4), IDUTPU(5), IPOINT(5)
COPMEN/UNCON/IFM4, IFCST, ITARG, IOPCW, IBIT, IPARS, IDATAS, IHW, MAXCOR,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        CCRYCALUNCONZIEWA, IFDST, ITARG, IOPCW, ISIT, IPARS, IOATAS, IHW, MAXCOR, LUCG, MPGS, TIMEC, NRCORS, NSTAT, LBPSI, LBPSZ, NULL, IONE, IT,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          ECUIVALENCE (ISYSMK, ISPM(26)), (IPRMSK, ISPM(27)), (IAMP, ISPM(29)),
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CONYCHIONCENTIFHA, IFOST, ITARG, IOPCH, INIT: IPARS, I DATAS, IHM, MAXCOR,
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                                                   CUIVALENCE (ISYSMK, ISPM(26)), (IPRMSK, ISPM(27)), (IAWP, ISPM(29)),
LOCG, MPGS, TIMBG, NRCGCE, NSTAT, LBPS1, LBPS2, NULL, IONE, IT.
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                                      CMMON / DVAR/ ICPCO(255), ITCNTR, IOFFST, IOPRNO(3), ISTAT
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RETURN
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151 RETURN   STORE=11.70  511 END   STORE=11.70  512 FUNCTION JEXEIN(18UF, IST, ILNG)   FUNCTION JEXEIN(18UF, IST, ILNG)   FUNCTION JEXEIN(18UF, IST, ILNG)   CONVERTS CHAR STRING IN FEX - INTERNAL, 7094, TO   STRING LOC   STRI	2309	• :	I CST-IS, IN, IHOST-IN, ISOR	
END  STEFT GCRO27 CFCK  CONVERTS CHAR STRING IN FEX - INTERNAL 7094 TO  CONVERTS CHAR STRING IN FEX - INTERNAL 7094 TO  CONVERTS CHAR STRING IN FEX - INTERNAL 7094 TO  CONVERTS CHAR STRING IN FEX - INTERNAL 7094 TO  CONVERTS CHAR STRING IN FEX - INTERNAL 7094 TO  CONVERTS CHARS  CONVERTS CHARS  CONVERTS CHARS  CONVERTS CHARS  CONVERTS CHARS  CONTROL IS NR CF FEX CHARS  INTEGER 13UF 100  CONVERTS CHARS  LOUPPO CONTROL  CONT	2010		ISTORE=IIV	-
13. \$18FTC CCR027 CFCK  13. CCR027 CFCK  14. CCR027 CFCK  15. CCR027 CFCK  15. CLAR STRING IN FEX - INTERNAL 7094 TO  15. CCR02 CLOC  15. CCR02 CLOC  15. CCR02 CLOC  15. CCR03 CCCCCCC  15. CCR03 CCCCCCCC  15. CCR03 CCCCCCCCC  15. CCR03 CCCCCCCCCC  15. CCR03 CCCCCCCCCCC  15. CCR03 CCCCCCCCCCCCC  15. CCR03 CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC	2012	;	ENO	
CCNVERTS CHAR STRING IN FEX - INTERNAL 7094 TO  15 C 18	2013	\$ 1.8 B.	INCTABLE 1ST. ILNG)	
016 C 18UF IS STRING LOC 017 C 1ST 1S PTR TC 1ST CHAR IN 18UF 018 C 1LNG IS NR CF HEX CHARS 019 CCMMCN/BUF1/ 18UF 020 CATA 15083/C60606060606060 021 LHOST=36 022 K=0 024 IBUMP=0 025 L=IST+ILNG 025 L=IST+ILNG 026 CO 501 I=1,1LNG 027 CUMP=18UF(M) 028 P=L-1 039 ICUMP=1ECAS(15UMP+1FCST+6) 031 K=K+1 032 ICUMP=1CAS(15UMP+1FCST+6) 033 IF(11UMP=0) 034 IF(11UMP=0) 035 IF(11UMP=0) 037 CONTINUE 035 IF(11UMP=1CAS(15UMP+1FCST+6) 037 CONTINUE 037 CONTINUE 038 RETURN 037 CONTINUE	2015		S CHAR STRING IN HEX - INTERNAL 7094 TO	
116 C	2016		STRING LOC	-
019 INTEGER 18UF(80) 020 CCMMCN/BUF1/ 18UF 021 IHOST=36 022 K=0 024 IBUMP=0 025 L=1ST+1LNG 026 CG 501 I=1,1LNG 027 ICUMP=0 028 M=L-1 1CUMP=0 039 ICUMP=1EUF(M) 1F(ICUMP-EC,15088) GG TC 56 030 IF(ICUMP-EC,15088) GG TC 56 030 IF(ICUMP-EC,15088) GG TC 56 031 K=K+1 032 ICUMP=1LCAS(1CUMP,1FCST,5) 034 IF(ICUMP-GT,9) ILUMP=1LUMP- 035 ICUMP=1AUMP+1CMMP+1EUMP- 035 ICUMP=1AUMP+1CMMP+1EUMP- 035 IF(ICUMP-GT,9) ILUMP=1LUMP- 035 IF(ICUMP-GT,9) ILUMP=1LUMP- 035 ICUMP-GT,9) ILUMP=1LUMP- 035 IF(ICUMP-GT,9) ILUMP=1LUMP- 035 ICUMP-GT,9) ILUMP-GT,9) ICUMP-GT,9)	2018	;	NR OF HEX CHARS	
0220	2019		•	
1HCST=36  X=0  1AUMP=0  1AUMP=0  025  L=IST+ILNG  027  1LUMP=10   I=1, ILNG  029  ICUMP=1BUF(M)  1F(ICUMP=5C.150BB) GO TC   SO  030  1F(ICUMP=1CAC(1CUMP+1FCST,6)  1F(ICUMP=1CAC(1CUMP+1CST,6)  031  IF(ICUMP=1CAC(1CUMP+1CST,6)  032  1CUMP=1CAC(1CUMP+1CST,6)  033  1F(ICUMP=1CAC(1CUMP+1CST,6)  034  1AUMP=1CAC(1CUMP+1CST,6)  035  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  037  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CST,6)  1AUMP=1CAC(1CUMP+1CMP+1CMP+1CMP+1CMP+1CMP+1CMP+1CMP+1C	2020		/euri/	
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120MP=0 L=IST+ILNG 026 D0 501 I=1,ILNG 028 ILUMP=0 030 IF(ILUMP=1EUF(M)) IF(ICUMP,EC,ISOBB) G0 TC,S0 031 IF(ICUMP,EC,ISOBB) E0 TC,S0 032 ILUMP=ILCAS(ICUMP,IFCST,6) 034 IF(ILUMP=ILCAS(ICUMP,IFCST,6) 035 IF(ILUMP=ILCAS(ICUMP,IFCST,6) 036 IF(ILUMP=ILCAS(ICUMP,ICUMP-I	2324		18UMP=0	
027	2025			
1 LUMP=0 029 1 LUMP=1 BUF(M) 030 1 F(ICUMP=1ECAS(ICUMP,IECST,6) 031 1 K=K+1 1	2323		"   C	
0.23 0.33 1 F(ICUMP.SC.15088) GO TC.50 0.32 1 LUMP = ILCAS(ICUMP, IECST,6) 0.34 1 F(ILUMP.GT.9) ILUMP = ILUMP = ILUMP = 1LUMP =	2028 2028			
031	2030	;	BUF(M)	
033   LUMP=ILCAS(ISUMP,IESST,6) 034   IF (ILUMP,GT.9)   ILUMP=ILUMP- 035   IAUMP=ILUMP+ILUMP+ICMP+ 035   GONTINUE 037   SGI   GONTINUE 038   RETUPN   R	2031		P.EC.15088) GO TC,5	
035 IAUMP=IAUMP+IAUMP+16**(K+1 036 SOI CONTINUE 037 SOI CONTINUE 037 SETUPA 038 RETUPA	2033		LCAS(ICUMP,IESST.6) P.67.9) ILUMP=ILUMP-	
0.3.7 General Control	2033	y V	10v2+1UNP+16**(K-1	-
23.5 RETUR	7337	<u>ن</u>	EXEIN-ILON	:
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COMMON/UNCON/IFWA, IHOST, ITARG, IOPCW, IBIT, IPARS, I DATAS, IHW, MAXCOR,
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200 REEL 1701, 441, 45 COT COT COT COT COT COT COT COT COT COT	* \ * \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	ECK FCR PRESENCE/ABSENCE OF MEMORY ADDRESS-KI	
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C CHECK FOR PRESINCE/ABSENCE OF REGISTER ADDRESS-KEYED SNAP.  C DOT SEAL TOOL PASSING TO 2008  BE CONTRACTOR TO 2008  C DOTS READ CONTRACTOR TO 2008  C DOTS READ CONTRACTOR TO 2008  C DOTS READ CONTRACTOR TO 2009  C DOTS R	* * 0 1	***	
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C C C C C C C C C C C C C C C C C C C		ECK FL. PRESENCE/ABSENCE OF MEMORY OPER	
2008 READ 1001,MOSNAP  B	* * > O		
FILENDT.MOSNAP  GO TO 2009   READ 1002; NMCSK	7. 2008 R	AD 1001, MOSNAP	· · · · · · · · · · · · · · · · · · ·
CO 006 1=1,NPGSK  REAC 1607,NDSK411),NMOSKL(1)  1007 FORMAT(16,011,14)  JJ=NPGSKL(1)  CO6 REAC 1003,(MCSLGC(1,J),J=1,JJ)  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE OF REGISTER OPERA  CC CHECK FCR PRESENCE/ABSENCE/ABSENCE/	<b></b> 0	(*NOT.MOSNAP) GO 10 200	
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COO READ 1003, (MCSLGC(I,J),J=1,JJ)  COO READ 1001, RGSNAP  C * * * * * * * * * * * * * * * * * *	2 1007 F	RMAT(16,011,14)	
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1	* * U	SICK FOX PRESENCE/ABSENCE OF REGISTER OFICEA	
1 IF(.NCT.RCSNAP) GG TG 2C01  READ 1001, RCSNAP) GG TG 2C01  READ 1002, NRCSK  CC 007 I=1, NRGSK  AJ=NRCSKL(I)  JJ=NRCSKL(I)  C CT READ 1007, RCSLGC(I,J), J=1,JJ)  A C C CONPERTURN  SLUBRCUTINE SNAPEX  C C C N N N N N N N N N N N N N N N N	ن		
FIGURE   1007   11   1   1   1   1   1   1   1   1	0 2009 R	AD 1001, RGSNAP	• ;
CC 007 I=1,NROSK  READ 1007,RCSK4(I),ROSK(I),NROSKL(I)  JJ=NRCSKL(I)  COT READ 1003,(RCSLGC(I,J),J=1,JJ)  C 2001 RETURN  S 2001 RETURN  S 1004CUTING SARPEX  C C 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	- a.	ACTIONS NECESTARY OF THE SECTION OF	
READ 1907, RGSKA(1), NROSKL(1)  JJ=NRCSKL(1)  6 COT READ 1603, (RCSLGC(I,J), J=1,JJ)  7 C  201 RETURN  4 IFFIC SNAPSR DECK  2 C SUBRUTINE SNAPEX  C C C C C C C C C C C C C C C C C C C	3	007 I=1,NROSK	
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PCSNAP, OCSNAP, TSNAP, LTSNAP (9), MASNAP, RASNAP, MOSNAP, ROSNAP
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 COMMENJUNCON/IFWA, IFOST, ITARG, IOPCM, IBIT, IPARS, IDATAS, IHW, MAXCOR
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                CESIRED MM LOCATIONS
                                                                                                                                                                                                                                                                                                                                                                                                                                                                           IINSPAR(5,23), IPCTR(5), IPPCTR(5), ISGCD(5,20), IADR(3), ISPM(64),
                                                                                                                                                                                                                                                                                                                                                                                                                                                              CCMMCN /UARRAY/ ISECTA(20).TIME(10).CLASS(10).INSDAT(256.5).
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    AND APPROPRIATE VARIABLES
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 EFFECT.)
                                                                                                                                                                                                                                                                                                          MOSNAP,NMOSK,MOSKA,MOSK,NMOSKL,MOSLOC,
ROSNAP,NROSK,ROSKA,ROSK,NROSKL,ROSLOC
                                                                                                                                                                                                                                                                                                                                                                          I LOCG, MPCS, TIMBC, NRCOEE, NSTAT, LBPS1, LBPS2, NULL, IONE, IT,
                                                                                                                                                                                                      TISNAP, STI, SSTRT, SSTPT, NTISNA, TISLOC
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 IS IN
                                                                                                                                                                                                                                                                                         TSNAP, NTSK, TSK, NTSKL, TSLUC, LTSNAP
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                FORMAT(1H0,5X,11HMM_LGCATION,7X,14HOCTAL_CONTENTS)
                                                                                                                                                                                                                       /KS/KSNAP, PCSNAP, NPCSK, PCSK, NPCSKL, PCSLOC,
                                                                                                                                                                                                                                         CCSNAP, NGCSK, OCSK, NOCSKL, GCSLOC,
                                                                                                                                                                                                                                                         MASNAP, NMASK, MASK, NMASKL, MASLOC,
                                                                                                                                                                                                                                                                          RASNAP, NRASK, RASK, NRASKL, RASLOC,
                                                                                                                                                                                                                                                                                                                                            ICPCO(255), ITCNTR, IUFFST, IOPRND(3)
                                                                                                                                      MOSKA(9),MOSK(9),NMCSKL(9),MOSLOC(6,9)
RCSKA(9),ROSK(9),NKOSKL(9),ROSLOC(6,9)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             FORMAT(1H3,45H A FULL SNAP CIAGNOSTIC ROUTINE
                                TEGER SLGC(9), TISLOC(9), NTSKL(9), TSLOC(5,9)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                SNAP DIAGNOSTICS AR
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                                                                                    CCSK(9), NOCSKL(9), CCSLOC(9,9),
                                                                                                    MASK (9), NMASKL (9), MASLOC (9,9),
                                                                                                                      RASK(9), NRASKL(9), RASLOC(5,9),
                                                                     INTEGER PCSK(9), NPCSKL(9), PCSLOC(9,9),
                                                                                                                                                                                                                                                                                                                                                                                             OSLAE, ILC, INTODE, ICOUNT, EXTIME, TIMLIM,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    TIME INTERVAL SNAP KEY IS CHECKED
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               11H4LFW(5), 1STACK(5,6), IMAINM(4096)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   UPCATEC IF A SNAP IS PERFORMED.
                                                                                                                                                                                      CCMMON / FS/SNAP, FSNAP, NFSL, SLOC,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  #
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                CUIVALENCE (INACOR, ISPM(25))
LCGICAL FSWAP, TISWAP, KSNAP,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     IF(SSTAT-TIPEC) 197,107,106
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                                                                                                                                                                                                                                                                                                                                                                                                                               LOBOUN, JIECUN, MONE, IFETC
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 IF (.NCT.FSNAP) GG TC 100
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                IF A FULL SNAP CIAGNOSTIC
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                                                                                                                                                                                                                                                                                                                                                                                                            IINW, IMN, LERFLG, IRESTA,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    WRITE(6,105) II, III
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               (II) KNITHI = III
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52 C * * * * * * * * * * * * * * * * * *		
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403 IF((.NOT.RASNAP).ANG.(.NOT.MASNAP).AND.(.NOT.ROSNAP).AND.(.NOT.ROSNAP).AND.
                                                                          , F12.3,6H MSEC.
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                                                                                                                                                                                                                                                                                                                                                    CHECKED
                                                                        PROGRAM
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                                                                                                                                                                                                                                                                                                                10 (437,407,407,407,408,408),13
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                                                                                                                                                                                                                                                                                                                                                                                                      TO 305
                                                                                                                                                                                                                    BRANCH TO APPROPRIATE LOGIC
         IF(.%CT.LTSNAP(I)) GO TO 404
                    F(TIMBE-TSK(II) 404,405,405
                                                                                                                                                                                                                                                                                                                                                    ACCRESS KEY
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                                                                        FORMAT (1HO, 35H TRIGGERED BY
                                                                                                                                                                                                                                                                                                                                                                                                      IF (RASK(1).NE.ISEGTA(2)) GO
                                                                                                                                                                                                                                                                                                                                                                                                                                                 FURMAT(1HO,31H TRIGGERED
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 IF(.NCT.RCSNAP) GC TC
                                                                                                                                                                                                                                                                                           IF(1).LT.1) GC TO 4C9
                                                                                                                                                                                                                                                                                                                                                                                                                                      WRITE(6,115) RASK(1)
                                                               WRITE(6,114) TSK(I)
                                                                                                                                                           WRITE(6,105) II, III
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     WRITE(6,105) II, II
                                                                                                                                                                                                                                                                                                                                                   REGISTER CPERANC, 1
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                               TSNAP(I)=.FALSE
                                                                                                                                                                                                                                                              1NAP)) GC TO 439
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                                                    WRITE(6,125)
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                                                                                                MRITE(6.124)
                                                                                                          RRITE(6,134)
                                                                                                                                CC 476 J=1,K
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                                                                                     CALL PEACER
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FIRESKALLISECTALBY OF TO 308
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                                                   GC TO (409,413,413,408,408,408),1J
                                                                                                                                                                                                                                                                                                                                           FIRESK(1).NE.15PM(1MN1) GQ TQ 3G8
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                                                                                                                                  IFIRASKII) . NE . ISEGTAL 3) 1 GO TO 3C7
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PCTRAC, CCTRAC, TTRACE, LTTRAC (9), MATRAC, RATRAC, MOTRAC, ROTRAC
                                                                                                                                                                                                                                                FORMAT(1H), 29H TRIGGERED BY MEMORY OPERAND ,011,13H AT LOCATION
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        /KI/PCT9AC, NPCTK, PCTK, NIPCTK, OCTRAC, NDCTK, OCTK, NIGCTK,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          NGTKA(S), NOTK(S), NINOTK(9), ROTKA(S), ROTK(9), NIROTK(9)
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                NTEGER PCTK(9), NIPCTK(9), GCTK(9), NIOCTK(9), NITTK(9), MATK(9), NIMATK(9), RATK(9), NIRATK(9),
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                                                                                                                                                                                                  IF(MUSK(I).NE.ICPRNC(IIII)) GO TO 310
                                                                                                                                                                                      IF(MCSKA(I).NE.1ACR(IIII)) GG TG 310
                                                                                                                                                                                                                                                                                                                                                                                                              IF ((IIII.EG.2).AND.(IJ.EQ.6)) GO
                                                                                                                            CTECKED
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                                                                                                                                                               IF (.NCT.MCSNAP) GQ TO 494
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                                                                          WRITE(6,105) II, III
                                                                                                                           MEMORY OPERAND IIII
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                                                                                                                                                                            DG 310 I=1,NPCSK
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APITE(6,124)
                                       CC 417 J=1,K
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              *17f(6,134)
=NMASKL(1)
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TRACES ARE PRESENT, THE KEYS ARE READ ALONG WITH APPROPRIATE IS READ HERE IS READ HERE. ALLOWED APPROPRIATE DATA IS READ IF DIAGNOSTIC IS TOLLITHEETHETHETHE VARIABLE 13 ONLY TRACE CIAGNOSTIC ALLOWED. HE KEYECTRACE/NOKEYEC TRACE VARIABLE # # # # \* RESE . TABSENCE OF \*\*\* PRESENCE A PESENCE OF CHECK FOR PRESENCE/ABSENCE OF \* \* \* \* \* READ 1009, SCIK(I), NIPCTK(I) REAC 1013,0CTK(I),NIOCTK(I) SECTRACE SOLO 2010 2014 IF(.NCT.TITRAC) GO TO 2011 READ 1008, TRII, TSTRI, ISTPI TO 2012 TO 2013 NEAD INILITRATIONITER (1) IF ( NCT POTRAC) GO READ 1001, OCTRAC IF(.NCT.CCTRAC) GD IPL.NCT.TTPACEN GO \*\* REAC 1001, FTRACE IF (FTRACE) GC TC CIAGNESTIC CATA. C 404 I=1,NPCTK DO 405 I=1,NCCTK READ 1001,TITRAC READ 1001, TTRACE # # \*\*\* READ 1002, NPCTK 20 430 T=I+NTTK REAC 1002, NCCTK BITRAC(I) = TRUE GC 404 1-1-27FK FORMST (3F12.3) REAC 1002+1118 4 4 4 FURMAT (16,14) FORM 17 (14,14) FORMAT(15) CHECK FCR \* \* \* \* \* \* \* \* \* \* ø REAC 1. READ 4 **\$ \$** . H 1009 ---1010 011 404 **4** 2012 2013 400 . 1002 **\* # #** 1008 O 2775 2777 2778 2779 2730 2781 2782 2783 2784 2785 2786 2786 2787 2789 2789 2896 2897 2808 2809 CIHZ 2318 3319 2820 2821 2822 2823 ¥. -: 2774 2793 2794 2442 2798 2799 803 804 5005 313 2816 2017 7660 2791 2792 1.36 2737 0082 801 2312 7:62 2415 いんかん 911

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PCTRAC,CCTRAC,TTRACE,LTTRAC(9),MATRAC,RATRAC,MOTRAC,ROTRAC
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ADDRESSHKEYED
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                                                                                                                                                                                                                                                           CHECK FCR PRESENCE/ABSENCE OF MEMORY
人民の名は、中の一百つ人日の日本では人口の古の日本に
                                                                                                                                                                                                                                                                                                                                               READ 1012, MOTKA(1), MOTK(1), NIMOTK(1)
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                                                                                                                                                                                                                    READ 1010, RATK(I), NIRATK(I)
                                                                                      REAC 1009, MATKII), NIMATKIII
                                                                                                                                                                                 TO 2016
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                                       EAD 1001, MATRAC
IF(.NCT.MATRAC) GG
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                                                                             CO 407 I=1, NFATK
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                                                                                                                                                  IF A FULL TRACE CLAGNOSTIC IS IN EFFECT, THE REGISTER TRACE IS PERFORMED AND ANY CTHER TRACE DIAGNOSTICS ARE NOT ALLOWED.
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IF ((RATK(I) . EC. ISEGIA(2)) . ANC. (NIRATK(I) . GI. ITCNIR)) ITCNIR=NIRATK
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LITRAC(I)=.FALSE.

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753 FORMAT(1H2,12HSPM_LCGATION,1X,14HOCTAL_CONTENTS,3X,12HSPM_LOCATION
                                                                                                                                IF ((MCTKA(I). EC. IACR(IIII)). AND. (MOTK(I). EQ. IOPRUD([III]). AND. (NIM
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       1.1X.14HCCTAL CONTENTS.3X.12HSPM LOCATION.1X.14HOCTAL CONTENTS.3X.1
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   SPM REGISTERS
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LCGICAL POSPME,CCSPMD,TSPMD,LTDK(9),MASPMD,RASPMD,MOSPMO,ROSPMD
                                                                                                                                                                                                                                                                         ITCNTR IS A COUNTER INDICATING THE CURRENT NUMBER OF SUCCESSIVE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                POSTMO NYOCK PROKAFROSK, ROSPMO JAROUK •RODK 4-RODK
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    CURRENT (OCTAL) CONTENTS OF THE
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                                                                                                                                                                                                                                                                                                            TPACE HAS BEEN REQUESTED
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                                                  MEMORY CPERAND 1111
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CHECK FOR PRESENCE/ABSENCE OF REGISTER-ADDRESS-KEYED SPM DUMP.
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READ HER.
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                                                                                                                                                                                                                                                                                                                                                                                                               READ 1002,NCCCK
READ 1013,(GCCK(I),I=1,NOCCK)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    1013, (MACK(1), I=1, NMACK)
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                                                                                                                                                                                                     IF(.NCT.PCSPME) GC TO 2019
READ 1002,NPCCK
                                                                                                                                                                                                                                                                                                                                                                            READ 1001,0CSPMC
IF(.NCT.CCSPMC) GO TO 2020
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                                                                                IF(.NCT.SPMD) GO TO 2018
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READ 1013, (RACK
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                                                   READ 1001, SPMC
FORMAT(LS)
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CHECK FOR PRESENCE/ABSENCE OF MEMORY-OPERAND-KEYED SPM DUMP.

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, MASPING, NY ACK, MACK, RASPING, NRADK, RADK, TSPING, NTOK, TOK, LTOK
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              LOGICAL PCSPYC, CCSPKO, TSPMC, LTOK(9), MASPYO, RASPMO, MCSPYO, ROSPMO
  SPM DUMP
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             COMMON / UARRAY/ ISEGIA (20), TIME (10), CLASS(10), INSDAT(256,5),
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | INSPAR(5424) + | POTR(5) + | IPPOTR(5) + | SGCO(5,20) + | ADR(3) + | SPM(64)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         "MCSPMC, NWOCK, MOCKA, MOCK, ROSPMO, NROOK, ROOKA, ROOK
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            LGGG, MPCS, TIMBC, NRCOCE, NSTAT, LBPS1, LBPS2, NULL, IGNE, II,
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 COMMON /SP/SPMC, POSPMC, NPCCK, PODK, OCSPMD, NDCDK, OCDK
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                                                                                                                                                                                                                                                                                                                                                                                                                       CONFON
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       INTEGER PCCK(9), CCCK(9), MACK(9), RADK(9),
                                                                                                                                                                             READ 1015, (RCCK&(1), RCCK(1), I=1, NRODK)
                                                                                                                                                                                                                                                                                                                                                                                                                  CIMENSICA, SPM CUMP, VARIABLES, AND CEFINE
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           MODKA (9), MOCK (9), ROCKA(9), RODK (9)
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CHECK FCR PRESFNCE/ABSENCE
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                                                                                                                  IF ( *NCT * HCSPMC) GC TO 2018
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       LCBCUN, JI SCUN, MCNE, IFSTC
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SUBRCUTINE SPACEX
                                                                                        REAC 1001, RCSPMC
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                                                                                                                                                 1002, NRCCK
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FORMAT(1F0,12HSPM LGCATION,1X,14HOCTAL CONTENTS,3X,12HSPM LGCATION
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READ 1002, MELCK

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## APPENDIX V. SAMPLE PROGRAM OUTPUT

This appendix contains a sample program printout which illustrates the various types of diagnostics and statistics which the SUMC simulator makes available to the user. The target program used in obtaining the printout consisted of diagnostic routines which are currently being used for checkout of the SUMC Breadboard System instruction set.

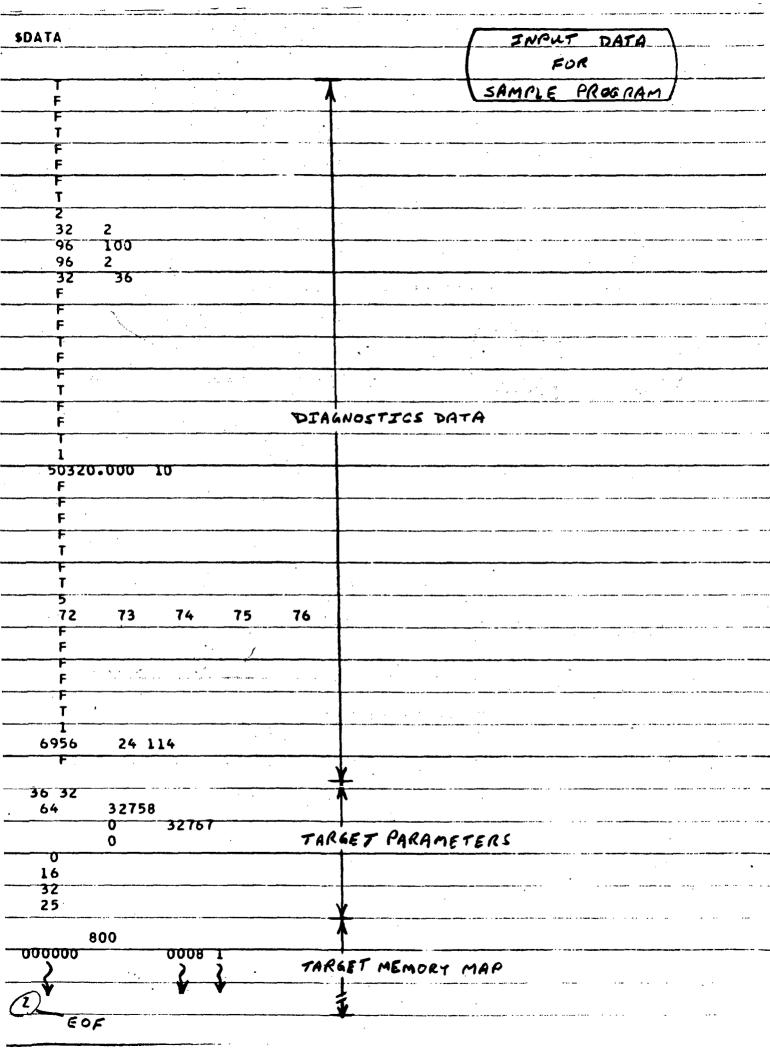
The sample program includes the following types of diagnostic printouts:

- TRACE A time-keyed TRACE diagnostic was requested such that a printout of the contents of key target computer registers is obtained at simulated elapsed time 50320.000 msec and the TRACE would remain in effect for ten consecutive instructions.
- SPM DUMP An op-code-keyed scratch pad memory dump was requested such that any halfword operations encountered during the simulation would trigger a dump of the contents of SPM prior to the instruction execution. The current SUMC instruction set includes five instructions which specify halfword operations; those are LH, CH, AH, SH and MH and their op codes are (hexadecimal) 48, 49, 4A, 4B and 4C, respectively.
- SNAP A memory-address-keyed SNAP diagnostic was requested such that any target instructions addressing MM location 32 or MM location 96 would trigger a printout of the contents of MM locations 96 and 100 or MM locations 32 and 36, respectively. In this case, SNAP locations were chosen so that both the old and new program status words could be checked when a Supervisor Call (SVC) instruction is executed.

BLOCK MM DUMP - A block dump of the contents of MM locations 24 through 137 was requested whenever the current value of the program counter was equal to 6956. This particular memory dump would allow the user to check current values of program status words residing in main memory.

The standard statistics table is shown at the conclusion of the program printout and the following information is supplied concerning the target program which has been simulated:

- Number of instructions of various classes which were executed.
- Time used in executing each class of instruction.
- Percentage of total time used in executing each class of instruction.
- Total number of target instructions executed.
- Total simulated elapsed time.



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32	PRUGRAM IS AT OFFSET 229003 FROM FIRST EXECUTABLE IN	5015.000 MSEC.	THE CURRIMT INSTRUCTION ABURESS(PCOUNTER) IS 6964	CUARENT TASTRUCTIO+(14 OCTAL HALFWORDS) IS 95400	0.2 (1710CTAL) 539	32 IS(OCTAL) 377	SHAPPED LOCATIONS AND THEIR (OCTAL) CONTENTS ARE	4TENTS	00000	3609600000	LON	TIME	29890.0	170.5	1786580.)	320.0	0.0-	120.3	20.0	1145205.0
TRIGGERED BY MEMORY ADDRESS	OFFSET 229003 FR	SIMULATED ELAPSED TIME IS 1145015.000 MSECT	NSTRUCTION ADDRESS	ASTRUCTION (IN OCT)	REGISTAR OPERANO 1 AT SPA ADDRESS	D 1 AT MM ADDRESS	OCATIONS AND THEIR	0.1 OCTAL CONTENTS	00001000000	0660060000	INSTRUCTION CLASS DISTRIBUTION	COUNT	2959.0	17.0	0.809871	52.0	6.6-	12.0	2.0	223341.0
TRIGGERED BY	PRUGRAM IS AT	SIMULATED ELA	THE CURRIST !	THE CURRENT I	AGISTAR OPER	MEMORY OPERAND 1	THE SNAPPED L	WM LOCATION	96	COT TOO	TASTRUCTIO	CLASS	/- (·		i iņ	c ~-	• व्ह		<u>C</u>	

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